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Research Article

Tunable 1/*f* Noise in CVD Bernal-Stacked Bilayer Graphene Transistors

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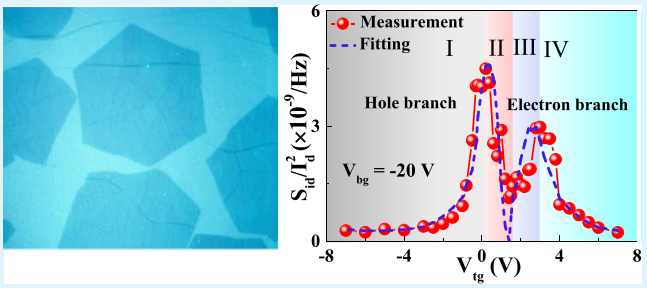
ABSTRACT: Low-frequency noise is a key performance-limiting factor in almost all electronic systems. Thanks to its excellent characteristics such as exceptionally high electron mobility, graphene has high potential for future low-noise electronic applications. Here, we present an experimental analysis of low-frequency noise in dual-gate graphene transistors based on chemical vapor-deposited Bernal-stacked bilayer graphene. The fabricated dual-gate bilayer graphene transistors adopt atomic layer-deposited Al_2O_3 and HfSiO as top-gate and back-gate dielectric, respectively. Our results reveal an obvious M-shape gate-dependent noise behavior which can be well described by a quantitative charge-noise model. The minimal area normalized noise spectral density at 10 Hz reaches as low as about 3×10^{-10} $\mu m^2 \cdot Hz^{-1}$ at room temperature, much lower than the best results reported previously for graphene devices. In addition, the observed noise level further decreases by more than 10 times at temperature of 20 K. Meanwhile, the noise spectral density amplitude can be tuned by more than 2 orders of magnitude at 20 K by dual-gate voltages.



KEYWORDS: *Bernal-stacked bilayer graphene, dual-gate transistors, 1/f noise, charge-noise model, low temperature*

INTRODUCTION

Bernal-stacked bilayer graphene (BLG) is a unique two-dimensional semiconductor whose band gap can be tuned by the electric-field-induced broken layer symmetry, making it a promising candidate for electronic applications.[1,2] Significant progress on high-performance Bernal-stacked BLG devices has been made including radio frequency transistors with high voltage and power gain, high-gain active mixers, and low-loss resistive mixers.[3−5] Among these applications, low-frequency noise or 1/*f* noise plays an important role in the device performance and can become a potential performance-limiting factor. As an example, the 1/*f* noise can upconvert to higher frequencies by the inherent nonlinearities in field-effect transistors (FETs) and circuits, which can be the main contribution to phase noise of communication systems and sensors.[6,7] To date, the 1/*f* noise in graphene devices has been studied extensively, and in some cases, the BLG material shows an order of magnitude reduction in noise level compared to that of monolayer graphene (MLG).[8−11] However, most of the above reports are based on the back-gate device structure. Dual-gate device geometry, which is the backbone for practical Bernal-stacked BLG device application, is still largely lacking. Pal and Ghosh[12] reported a V-shape gate bias dependency noise characteristic in dual-gate BLG device where polymethylmethacrylate (PMMA) and mechanically exfoliated BLG were used as top-gate dielectric and channel material, respectively. Heller et al.[10] developed a charge-noise model to explain M-like shape noise characteristics in mechanically exfoliated MLG and BLG devices where ionic liquid was used as top-gate dielectric. Furthermore, Kumar et al.[13] performed noise measurements in dual-gate hBN−BLG−hBN device, and they found that the gate bias dependent noise characteristic was Λ shape in primary Dirac cone. What we can see is that the gate bias dependence of noise characteristics is very different with different dual-gate dielectrics, indicating the obvious influence of interface characteristics on the noise measurements. On the one hand, dual-gate BLG devices fabricated by mechanically exfoliated BLG are known to suffer from low yield and uncontrollable size, which are serious technological bottlenecks for large-scale applications. On the other hand, growing the gate dielectric by atomic-layer-deposition (ALD) method on top of graphene is highly desired for large-scale applications. The noise characteristics in BLG devices with CVD-grown Bernal-stacked BLG as the channel material and ALD-grown dual-gate dielectrics is limited and has yet to be reported. In this work, we have conducted a thorough study of noise characteristics in dual-gate Bernal-stacked BLG devices

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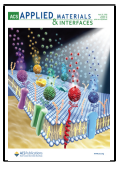

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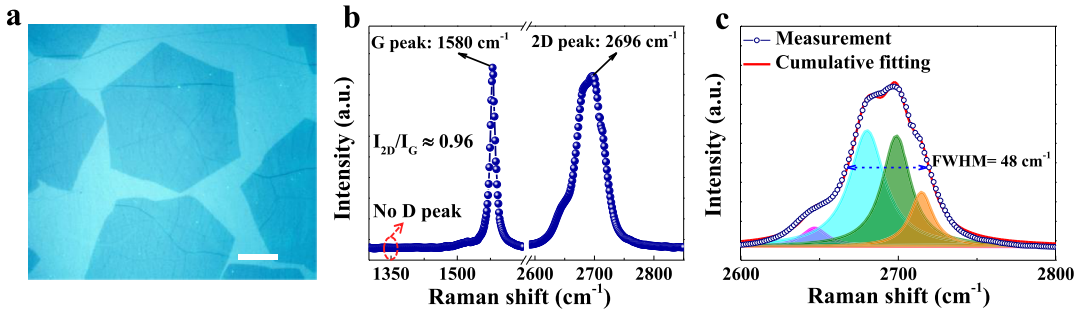

Figure 1. (a) Optical images of the BLG domains transferred onto HfSiO (14 nm)/SiO_2 (90 nm)/Si substrate. Scale bar: 40 μm. (b) Raman characterization of the BLG with the excitation laser of 532 nm. (c) 2D peak fitted by four Lorentzian peaks.

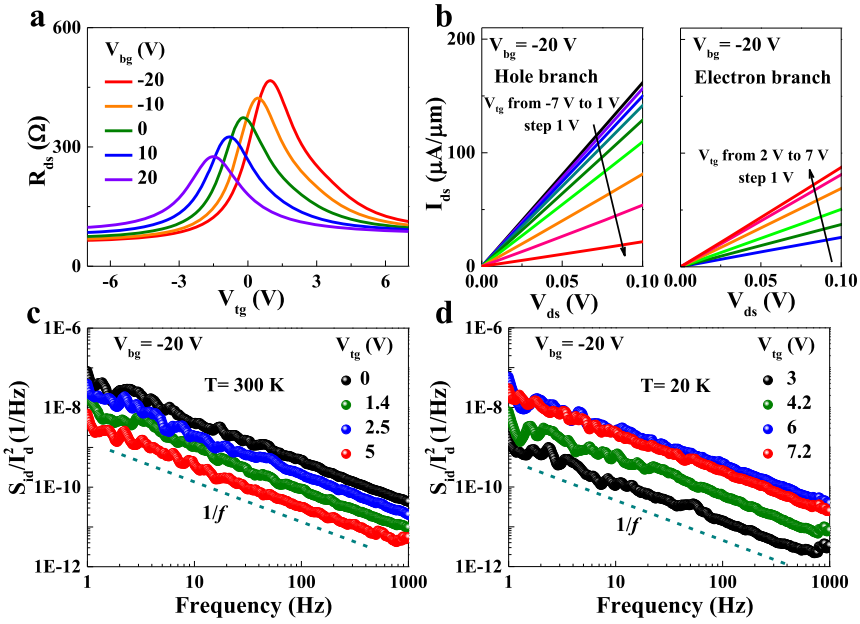

Figure 2. (a) Room temperature resistivity as a function of V_{tg} at different V_{bg} for the BLG FET with a gate length of 0.3 μm. The V_{ds} is fixed at 0.1 V. (b) Output characteristics of the same device in (a) at V_{bg} = −20 V. (c), (d) Low-frequency noise-normalized spectra S_{id}/I_d^2 as a function of frequency for several V_{tg} at T = 300 and 20 K, respectively. The V_{ds} is also fixed at 0.1 V. The ideal $1/f$ behavior is added for comparison.

with CVD-grown Bernal-stacked BLG as the channel material. Meanwhile, ALD-grown Al_2O_3 and HfSiO are adopted as top-gate and back-gate dielectric, respectively. We find that top-gate voltage-dependent $1/f$ noise exhibits an M-like shape, which is different from most other reported V-shape gate-bias dependence in BLG devices[8,10,12,14] This M-shape gate bias dependency is well explained by a charge-noise model, where the noise can be attributed to charge fluctuation in close proximity to the graphene at low carrier density and scattering in the graphene channel at high carrier density.[10,15] In addition, the minimal area normalized noise spectral density at room temperature reaches as low as about 3×10^{-10} $\mu m^2 \cdot Hz^{-1}$ at 10 Hz, 10 times lower than most of the reported results in the literature.[11,16−18] Furthermore, the noise performance at low temperature has been also demonstrated. The observed noise level decreases more than 10 times and can be tuned by about 200-times of magnitude by changing the dual-gate voltage at temperature of 20 K.

EXPERIMENTAL AND RESULTS

The Bernal-stacked BLG domains were grown using CVD technique by the thermal decomposition of CH_4 gas in the presence of H_2 gas on a copper foil pocket.[19,20] For a typical growth process, the copper pocket formed by folding a 25 μm thick copper foil was loaded into a 3 in. quartz tube inside a horizontal tube furnace. A gas mixture of 0.5 sccm CH_4 and 60 sccm H_2 flowed across the copper pocket at a temperature of 1070 °C for 2 h, after which the chamber was cooled to room temperature. The detailed BLG growth and transfer procedures are described in our earlier work.[4] In this way, the BLG film transferred onto HfSiO (14 nm)/SiO_2 (90 nm)/Si substrate is shown in the optical microscopy image of Figure 1a. The 90 nm SiO_2 layer is chosen for high visibility of BLG domains under optical microscopy. It has been proven that the high-k HfSiO dielectric with a dielectric constant of 18 contains low surface charge trap density and is expected to improve carrier mobility of graphene channel.[21,22] We can easily distinguish the BLG domains with an approximate hexagonal shape and clear uniform color contrast. The Raman spectrum was used to characterize the number of layers and the stacking order of the graphene. As can be seen in the Raman spectrum of Figure 1b, the peaks centered at 1580 and 2696 cm^{-1} correspond to the G and 2D bands, respectively. The intensity ratio between the 2D and G peak is about 0.96. No obvious D peak (centered at 1350 cm^{-1}, marked by red dotted part in Figure 1b) is observed in the Raman spectrum, indicating the high quality of the BLG film after being transferred onto the high-k dielectric interface. In Figure 1c, the full width at half-maximum (fwhm) of the 2D peak is 48 cm^{-1}. Meanwhile, the 2D peak with an obvious shoulder peak can be well-fitted by four Lorentzian peaks, which is consistent with the characteristics of Bernal-stacked BLG.[23] We further used atomic

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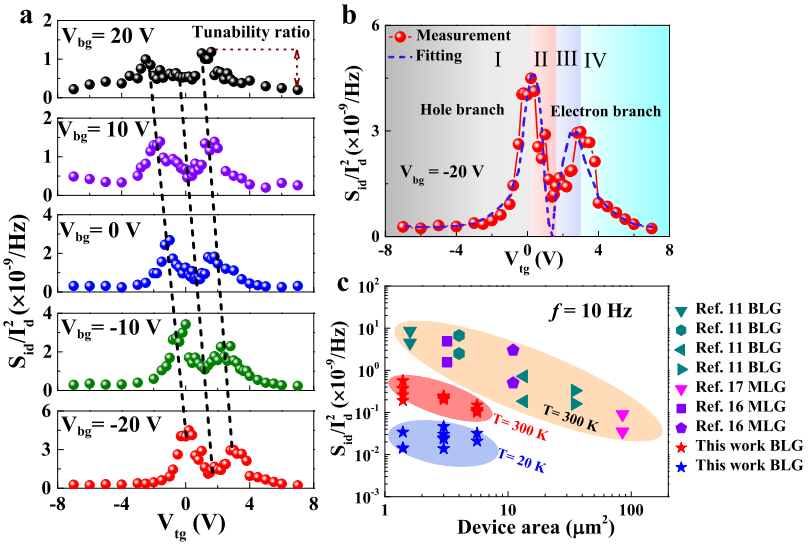

Figure 3. (a) Low-frequency noise-normalized spectra S_{id}/I_d^2 at f = 10 Hz versus V_{tg} at different V_{bg}. (b) S_{id}/I_d^2 at f = 10 Hz and V_{bg} = −20 V. The blue dot curve represents the result fitted by charge-noise model separately at $V_{tg} < V_{Dirac}$ and $V_{tg} > V_{Dirac}$ region. (c) Benchmark for S_{id}/I_d^2 at different device areas.

force microscope (AFM) to confirm the boundary between the BLG domain and MLG film. As shown in Figure S1a,b, the thickness of BLG is about 0.4 nm larger than that of MLG, which is close to the theoretical value of 0.34 nm. The high-quality BLG material provides the basis for the fabrication of BLG devices with low noise level.

After the BLG growth and transfer, BLG FETs with the dual-gate structure were fabricated using nanofabrication process.[4,5] The top gate dielectric consists of a natural-oxidized 2 nm Al seed layer followed by ALD-grown 15 nm Al_2O_3. The optical microscopy image and scanning electron microscopy image of the BLG device with two-finger configuration are shown in Figure S1c. Both of the back-gate and top-gate dielectric leakage current are less than 10 pA, as shown in Figure S2a,b. The room temperature resistance of a BLG FET with a gate length of 0.3 μm and gate width of 10 μm is shown in Figure 2a. The drain−source voltage (V_{ds}) is fixed at 0.1 V, while the top-gate voltage (V_{tg}) is swept from −7 to 7 V with fixed back-gate voltage (V_{bg}) varying from −20 to 20 V. The top-gate charge neutral points (CNPs) change linearly with V_{bg} related with a slope of about 1/16, as shown in Figure S2c, suggesting larger top-gate coupling strength and the gating efficiency. Similar to those observed in previous studies, tunable peak resistance at CNPs confirms the Bernal-stacked nature of the BLG under displacement electric field.[2,24] While at T = 20 K, the resistivity in CNPs increases and a positive shift in the CNPs is observed, as shown in Figure S4a. The positive threshold voltage shift can be attributed to the frozen trap charges at the oxide/BLG interface at low temperatures.[22,25] Figure 2b shows the output characteristics of the same device in Figure 2a at V_{bg} = −20 V for hole branch (left) and electron branch (right). The output characteristics at T = 20 K is shown in Figure S4b. It can be seen that both output characteristics for the hole and electron branches are highly linear at V_{ds} ranging from 0 to 0.1 V. Figure 2c,d shows the measured representative normalized noise spectra S_{id}/I_d^2 as a function of frequency at V_{bg} = −20 V for different V_{tg} at temperatures of 300 and 20 K, respectively. S_{id} is the current noise power spectral density and I_d is the drain current through the device channel, and the noise measurement method is similar to that in the literature.[17,26] The noise measurement setup is shown in Figure S3, where the DC biases are provided by Agilent B1500 and the signal source analyzer Agilent E5052B is used to measure the low-frequency noise spectrum together with the Agilent flicker noise system E4725A. It is notable that the noise spectra reveal no obvious traces of the generation-recombination noise. The measured S_{id}/I_d^2 is inversely proportional to the frequency, confirming the 1/f noise nature in the dual-gate Bernal-stacked BLG device.[27] Hooge's empirical relationship with $S_{id} = A_N I_d^2/f^\gamma$ is commonly used to characterize the 1/f noise in transistors, where A_N is noise amplitude and γ is a fitting parameter.[17] By fitting the measured data with this empirical relationship, all of the γ values are determined to be close to 1, as shown in Figure S4c,d, indicating that the 1/f noise in the dual-gate BLG device is caused by a collection of fluctuations in channel resistance with a wide distribution of time constant.[27]

To understand the noise mechanism in the dual-gate BLG devices, we studied the correlation of S_{id}/I_d^2 on dual-gate voltage. Figure 3a shows the dependence of S_{id}/I_d^2 on V_{tg} for different V_{bg} at f = 10 Hz and T = 300 K. The S_{id}/I_d^2 does not increase monotonically with changing V_{tg}. Instead, the S_{id}/I_d^2 exhibits a notable M-shape gate-bias dependence, where a local valley and two pronounced peaks are clearly visible. Meanwhile, the S_{id}/I_d^2 shows a weak gate-bias dependence at high V_{tg}. Notably, the V_{tg} values for these three special points change with changing V_{bg}, as shown by black dashed lines in Figure 3a. This variation approximately follows a linear relationship, which is the same as the linear relation between top and back gate voltages in BLG device CNPs, as shown in Figure S5a. This indicates that the charge fluctuations couple to the BLG transistor by effective top-gate and back-gate capacitance and the top-gate capacitive coupling dominates the noise characteristics.[10] This gate dependence of the S_{id}/I_d^2 can be explained by a charge-noise model, where the total noise power spectral density is described by $S_{id} = S_{input}(dI_{ds}/dV_{tg})^2 + \alpha_S I_{ds}^4$.[10,15] Among this expression, the $S_{input}(dI_{ds}/dV_{tg})^2$ term represents the noise associated with random charge fluctuations in the vicinity of channel−oxide interface and the $\alpha_S I_{ds}^4$ term represents the noise from a gate-independent noise source associated with scattering in the channel. Figure 3b shows a typical comparison of measurement and fitting results at V_{bg} = −20 V. The four different color regions labeled by I to IV in Figure 3b represent that the S_{id}/I_d^2 changes monotonically with V_{tg} at corresponding voltage intervals. The representative S_{id}/I_d^2 as a function of frequency at these four different bias regions is illustrated in Figure S6a−d. Given the conductance asymmetry, the hole and electron branches are fitted separately. We observe that the fitting result based on the charge-noise model matches the experimental result very well. As shown in Figure S5b,c, the fitting parameter for S_{input} at different V_{bg} are about 10^{-2} mV^2·Hz^{-1}, which is close to previous fitting result under the same BLG device area.[10] When the measurement temperature decreases to 20 K, the charge-noise model also fits the experimental result well, as shown in Figure S5d. It should also be noted that the S_{input} shows a slight increase but the α_S is 10 times lower than that of room temperature. This finding indicates that the

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ACS Appl. Mater. Interfaces 2020, 12, 17686−17690

noise associated with scattering in the channel is strongly suppressed at low temperature. Moreover, we use the coefficient of tunability ratio (defined on the top right corner of Figure 3a) as a feasible means to assess the capability of noise controlling by dual-gate voltage. The tunability ratio is more than 20 at $V_{bg} = -20$ V and increases with the increasing device on/off ratio, as shown in Figure S7a,b. The tunability ratio further increases to about 200 at $T = 20$ K, as shown in Figure S5d. The high tunability of $1/f$ noise will help design the future graphene-based devices with the best signal-to-noise ratio.[13] Figure 3c shows a benchmark for S_{id}/I_d^2 as a function of device areas with previous work. The noise data for our work is obtained from high V_{tg} region at different V_{bg}. As can be seen, the minimal area normalized S_{id}/I_d^2 at room temperature reaches as low as about 3×10^{-10} $\mu m^2 \cdot Hz^{-1}$ at 10 Hz, which outperforms most of the other graphene devices at the same frequency with the same device areas.[11,16−18] Also, the minimum area normalized S_{id}/I_d^2 further decreases to 1.5×10^{-11} $\mu m^2 \cdot Hz^{-1}$ at a temperature of 20 K. We note that the noise level is not strictly inversely proportional to the device area, which can be attributed to inhomogeneous BLG devices which are fabricated by different BLG domains.[11] The inhomogeneous BLG domains may result in spatial charge inhomogeneity and inhomogeneous trap distribution.[12,14,28] Finally, combined with noise characteristics in other literature,[10,12,13] it can be seen that whether the channel material is MLG or BLG, the gate bias dependency of the noise characteristics mainly rely on the interface characteristics between the graphene channel and gate dielectrics.

On the other hand, we calculate the noise amplitude from the measured normalized noise density using formula

$$A_N = \frac{1}{Z}\sum_{j=1}^{Z} f_j \left(\frac{S_{id}}{I_d^2}\right)_j$$

where $\left(\frac{S_{id}}{I_d^2}\right)_j$ is the normalized noise power density measured at the frequency f_j and $1 \le f_j \le 1000$ Hz.[16] This definition helps to reduce the measurement errors of the noise at specific frequencies and rule out other types of noise sources. Figure 4a,b shows the room temperature noise amplitude as a function of V_{tg} at different V_{bg} for device with $L_g = 0.3$ and 0.14 μm, respectively. It is clearly seen that the dependence of the noise amplitude on V_{tg} is also a clear M-like shape. Normally, the noise is known to increase with decreasing size.[29] The minimum noise amplitude increases with decreasing device areas, as shown in Figure S8a. The magnitude of noise reflects the ability of the conducting channel to screen the external potential fluctuations at the traps. As shown in Figure S8b, the minimum noise amplitude at $T = 20$ K is as low as about 3×10^{-10}, which is among the best values obtained in graphene devices so far.[8,9,12,13,30]

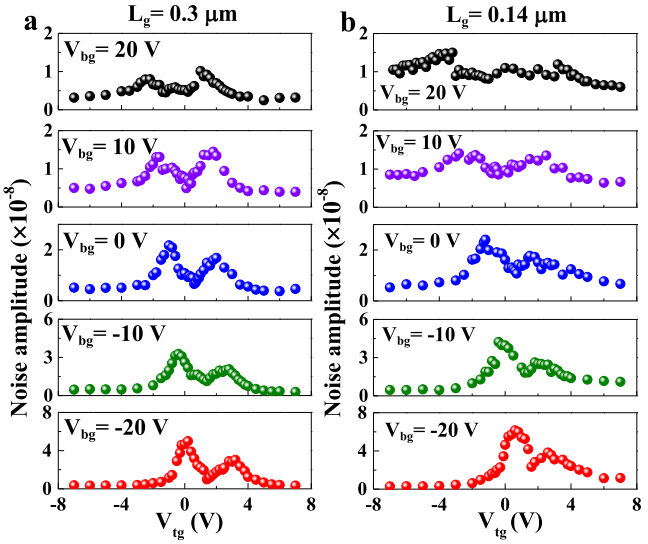

Figure 4. (a) Noise amplitude as a function of V_{tg} at different V_{bg} for device with $L_g = 0.3$ μm. (b) Noise amplitude as a function of V_{tg} at different V_{bg} for device with $L_g = 0.14$ μm.

CONCLUSIONS

In conclusion, we have studied the noise characteristics in CVD-grown Bernal-stacked BLG. Both of the top and back gate dielectrics in the dual-gate BLG FETs were deposited by the ALD method. The results show that the $1/f$ noise in the dual-gate BLG FETs exhibits an M-shape gate-bias dependence, which can be well explained by a charge-noise model. Furthermore, the BLG FETs exhibit the lowest noise level compared with previous results and can be reduced even further at low temperatures. Our results provide a coherent description of low-frequency noise in CVD-grown BLG materials, paving the way for its potential applications in the next-generation electronic devices.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsami.9b21070.

AFM image for the BLG film and the BLG device structure; detailed characterizations of top-gate and back-gate dielectric layers; noise measurement circuit; dc characteristics at $T = 20$ K and the fitting parameters of γ at all voltages; peaks positions in the M-shape gate-bias dependence characteristics and the fitting parameters of S_{input} and α_S at different V_{bg}; representative S_{id}/I_d^2 as a function of frequency at different bias regions; tunability ratio at different V_{bg} and on/off ratio; and dependence of noise amplitude on device areas and noise amplitude at $T = 20$ K (PDF)

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Notes

The authors declare no competing financial interest.

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