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ACS Appl. Mater. Interfaces, **Just Accepted Manuscript** • DOI: 10.1021/acsami.7b14031 • Publication Date (Web): 04 Dec 2017

Downloaded from http://pubs.acs.org on December 13, 2017

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Effect of Dielectric Interface on the Performance of MoS_2 Transistors

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ABSTRACT:

Due to their wide bandgap and ultrathin body properties, two-dimensional (2D) materials are currently being pursued for next-generation electronic and optoelectronic applications. While there has been increasing studies to improve the performance of MoS_2 field-effect transistors (FETs) using various methods, dielectric interface which plays a decisive role in determining the mobility, interface traps, and thermal transport of MoS_2 FETs has not been well explored and understood. In this paper, we present a comprehensive experimental study on the effect of high-*k* dielectrics on the performance of few-layer MoS_2 FETs from 300 to 4.3 K. Results show that the Al_2O_3/HfO_2 could boost the mobility and drain current. Meanwhile, MoS_2 transistors with Al_2O_3/HfO_2 afford a 2x reduction in oxide trap density compared to the devices with the conventional SiO_2 substrate. Also, we observe a negative differential resistance effect on the device with 1 μm channel length when using conventional SiO_2 as gate dielectric due to self-heating, and is being effectively eliminated by using the Al_2O_3/HfO_2 gate dielectric. This dielectric engineering provides a highly viable route to realizing high performance TMD-based FETs.

KEYWORDS: MoS_2, field-effect transistors, high *k*, pulse IV, low-frequency noise, negative differential resistance

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INTRODUCTION

After decades of ongoing progress, the silicon CMOS industry is approaching a stall in device performance for logic devices due to fundamental scaling limitations. To energize the future roadmap and enable continued dimensional scaling, novel materials with unique properties are being proposed to replace silicon substrate for lower supply voltage. Recently the rich family of transition metal di-chalcogenides (TMDs) MX_2, where M stands for a transition metal (Mo, W, Nb, Ta) and X for a chalcogenide atom (S, Se, Te), have received a lot of attention for their interesting properties[1-7]. Among them, molybdenum disulfide (MoS_2) is a representative semiconducting and has displayed interesting electrical, mechanical and optical properties due to a tunable bandgap of 1.2-1.8 eV and a reasonable mobility from 10-200 $cm^2/V \cdot s$ at room temperature[8-17]. Meanwhile, MoS_2 exhibits good thermal stability and could be grown by chemical vapor deposition in wafer-scale, providing the potential compatibility to silicon CMOS process[18-21]. Although great progress has been made in this field, challenges still remain to achieve high-performance MoS_2 transistors. The mobility of MoS_2 is still far below the theoretically predicted value, which is mainly limited by charged impurities and phonon scattering[22]. Studies have shown that the impurities and dielectric environment have an important impact on the electrical and optical properties of two-dimensional (2D) materials[23,24]. It is reported that hexagonal boron nitride (*h*-BN) is a promising dielectric material for MoS_2, which can significantly reduce charge traps and greatly enhance the electron field-effect mobility[25]. However, the BN flakes are irregularly shaped and are just a few tens of micrometers long, which is a roadblock to their practical use. It has been demonstrated that utilization of high-k dielectric materials as the gate insulator could partially screen charged impurities and improve carrier mobility[8]. Although much work has been devoted to study the interface between high-k/TMDs, most of them focus on the improvement in the transport properties such as mobility[26-31]. On the other hand, thermal conductivity (κ) of MoS_2 is very low and excessive heating can lead to poor device performance and

decreased lifetimes[32]. Using a high thermal conductivity material as the substrate could facilitate heat dissipation and relieve the self-heating effect[33]. In this work, we fabricated a dual-gated MoS_2 transistor to make a fair comparison for the back interface with SiO_2 and the top with Al_2O_3/HfO_2. Carrier transport, pulse *IV*, and low-frequency noise were comprehensively performed to investigate the effect of dielectric interface on the performance of MoS_2 transistors. Results show that, compared to the SiO_2 substrate, the Al_2O_3/HfO_2 could enhance the mobility and improve drain current as well as more effectively eliminate the self-heating effect. Our experimental work demonstrates a promising approach to improve the performance of MoS_2 transistors through substrate engineering.

RESULTS AND DISCUSSION

We start from mechanical exfoliation from commercially available bulk crystals. Figure 1a, b show the schematic of the MoS_2 device before and after atomic layer deposition (ALD), respectively. We deposited Al_2O_3 at 75 ºC to avoid pinholes and nonuniformity in the film. The thickness of MoS_2 used in this work is 4.2 nm, as shown in the inset of Fig. 1c, measured by atomic force microscopy (AFM). The channel length and width of the MoS_2 transistor are 1 and 4.2 μm, respectively. All the measurements were carried out under vacuum (< 10^{-5} Torr) in a Lakeshore cryogenic probe station using an Agilent parameter analyzer B1500A. The low-frequency $1/f$ noise measurements were carried out by Agilent B1500A and E5052B with a resistor unit.

We first study the effect of Al_2O_3/HfO_2 capping on the electrical properties of MoS_2 transistors. Figure 2a shows the I_d-V_g curves of back-gate MoS_2 before and after Al_2O_3/HfO_2 deposition. As shown in the inset of Fig. 2a, it is clear that the threshold voltage V_{th} shifts toward negative values of around 6 V due to the doping of Al_2O_3/HfO_2[27,28], suggesting a doping density of 1.4 $\times 10^{12}$ cm^{-2}.

Figure 2b shows the transfer characteristics of the back-gate and top-gate MoS_2 transistors at V_d = 0.05 V. The threshold voltage of back-gate and top-gate FETs are -17.5 and -15.6 V, respectively. The negative V_{th} is mainly due to the doing effect from Al_2O_3/HfO_2. A well-behaved output characteristic of a 1 μm-channel-length MoS_2 transistor with 90 nm SiO_2 gate dielectric is demonstrated in Fig. 2c, exhibiting a maximum drain current of 188 μA/μm with V_d = 3 V and V_{bg} = 40 V at 300 K. For the top gate with Al_2O_3/HfO_2 gate dielectric, the maximum drain current is 290 μA/μm with V_d = 3 V and V_{tg} = 10 V when fixed V_{bg} = 0 V. The on-current drivability of the top device is higher than the back device with SiO_2 gate dielectric due to better interface quality as well as a high mobility. Figure 2e shows a comparison of drain current for back gate and top gate at various temperatures. It is clear that at all temperature the drain current of the top gate is larger than that of the back gate, indicating that high *k* dielectric is more effective to improve the performance of MoS_2 transistors. Figure 2f compares peak transconductance (g_m) for the back-gate and the top-gate MoS_2 transistors at V_d = 0.05 V from 300 to 20 K. The g_m increases with decreasing temperature for both devices. As expected at all temperatures, the g_m is always higher for the top-gate device. The field-effect mobility μ_{FE} is extracted in the linear region of the transfer characteristics according to the following equations $\mu_{FE} = g_m/(C_g E W)$ and ($E = (V_d - 2R_c I_d)/L$), where g_m is the transconductance, C_g is the gate capacitance, E is the transverse electric field in the channel, L and W are the length and width of the channel, respectively, I_d is the drain current, and R_c is the contact resistance[12]. The mobility of the SiO_2 and Al_2O_3/HfO_2 devices at 300 K are 55 and 81 $cm^2/V \cdot s$, respectively. This improvement in mobility could be attributed to the reduction of Coulomb scattering by dielectric screening[25], which implies that Al_2O_3/HfO_2 dielectric has greater potential to realize high-performance transistors with TMDS channel materials.

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It is well known that conventional DC characterization methods have charge trapping phenomena that occur during long measurements[34]. To minimize the effect of charge trapping and de-trapping, pulsed *IV* measurement is required to obtain the intrinsic electrical characteristics of the MoS_2 transistors[35,36]. DC I_d is compared with I_d measured using different pulse widths, as V_d is swept from 0 to 3.5 V with V_{bg} = -30 V at 300 K as shown in Fig. 3a. The pulse width is changed from 5 ms (blue) to 25 ms (magenta). At all V_{tg}, the drain current increases with shorter pulse width and the DC measurement has the lowest drain current. With increasing V_{bg} to 0 V, the corresponding I_d-V_d curves are shown in Fig. 3b. Similar to the case in (a), all the pulsed curves are higher than the DC curves. The more traps in the interface, the much drain current degradation ΔI_d[36]. To investigate the interface quality, we define that ΔI_d is the difference between the DC and the pulse measurements with 5 ms pulse width at V_d= 2 V. Figure 3c shows ΔI_d versus V_{bg} with various V_{tg} at 300 K. It is apparent that ΔI_d increases with increasing V_{bg} and the trend is independent of V_{tg}. Owing to the intrinsic n-type of MoS_2, electrons in the MoS_2 channel will be close to Al_2O_3/MoS_2 interface when the V_{bg} is negative and will move to near the SiO_2/MoS_2 interface for positive V_{bg}. ΔI_d is proportional to the magnitude of traps[36]. Hence, the change in ΔI_d shows that there are fewer traps in the Al_2O_3/MoS_2 interface indicating a better interface quality compared to SiO_2/MoS_2 interface. Figure 3d shows ΔI_d as a function of V_{tg} with different V_{bg} at 300 K for the same two devices in (c). Obviously, ΔI_d decreases with increasing V_{tg} irrespectively of V_{bg}. The explanation is similar to that in (c). For $V_{tg} < 0$ V, electrons accumulate near to the SiO_2/MoS_2 interface. For $V_{tg} > 0$ V, electrons approach to the Al_2O_3/MoS_2 interface. This result also shows that interface quality of Al_2O_3/MoS_2 is better than that of SiO_2/MoS_2.

Low-frequency 1/*f* noise is also important which limits the performance of electronic communication systems and sensors[37]. For example, low-frequency noise determines noise-to-signal ration in digital

electronic device and low-frequency noise can be upconverted to phase noise in oscillators[38]. Here, we performed the low-frequency noise measurement on the back-gate MoS_2 device and the top-gate MoS_2 device in the linear region with V_d = 0.2 V at 300 K. The noise spectra can be quantitatively characterized by $S_{id} = \frac{AI_d^2}{f^\gamma}$, where S_{id} is the current noise power spectral density, f is the frequency, I_d is the current through the device channel, γ is frequency exponent, and A is the noise amplitude[39,40]. We extract the noise amplitude A using

$$A = (1/N)\sum_{m=1}^{N} f_m S_{Im}/I_m^2 \qquad (1)$$

where S_{Im} and I_m are the noise spectral density and drain current measured at m different frequencies[41]. Figure 4a shows the normalized A of the back-gate and top-gate MoS_2 transistors as a function of carrier density at 300 K. The noise amplitude from the top gate improves more than 40% than that from the back gate for the same carrier density, indicating that the interface quality of Al_2O_3/MoS_2 is better than that of the SiO_2/MoS_2. To evaluate quantitatively the interface property, we estimate the oxide trap density (N_{ot}) using input-referred voltage noise spectral density S_{vg} at the threshold voltage (V_{th}) as shown in Fig. 4b. It can be seen that the top-gate exhibits a reduced noise, implying a lower oxide trap density. The previous studies have demonstrated that the dominant noise mechanism of few-layer MoS_2 transistor is number carrier fluctuation[12,42,43]. It is then possible to evaluate the oxide trap density using the following formula[44,45]:

$$S_{vg} = \frac{N_{ot} kTq^2}{\alpha f W L C_g^2} \qquad (2)$$

where q is the element charge, kT is the thermal energy, and α is the tunneling constant ($\alpha = 10^8$ cm^{-1} is used here). The trap depth z at which the traps in the oxide is measured is derived from the noise frequency using[46]:

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$$z = \frac{1}{\alpha} \ln \frac{1}{2\pi f \tau_0} \quad (3)$$

where the time constant τ_0 is often taken as 10^{-10} s. Based on Eqs (2) and (3), we extracted the oxide trap density profile for the back-gate and top-gate transistors. The depth z of both devices is 1.43-1.90 nm with the noise measurements in the frequency ranging from 10 to 1000 Hz. Figure 4c shows the oxide trap density as a function of depth for both devices. The N_{ot} of $7.7\times10^{19} – 1.1\times10^{20}$ $cm^{-3}eV^{-1}$ for the top-gate device is lower than that of the back-gate device (i.e., $1.2\times10^{20} – 2.0\times10^{20}$ cm^{-3} eV^{-1}). This result is well agreement on our observation from pulse *IV* and consistent with the previous reports[47,48].

To further demonstrate the advantage of Al_2O_3/HfO_2, we compare the output characteristic of the back-gate and top-gate MoS_2 transistors at 70 and 4.3 K. Figure 5a depicts the well-behaved output characteristic of the back-gate device using SiO_2 substrate with V_d sweeping from 0 to 4 V for four different V_{bg} at 70 K. At V_{bg} = 25 V, the maximum drain current is 375 µA/µm and the curve exhibits current saturation. With increasing V_{bg} further, the drain current increases accordingly and even shows the sign of negative differential resistance (NDR) effect when I_d is larger than 400 µA/µm due to self-heating effect, which is consistent with the previous studies[12, 49]. The saturation current degradation $\Delta I/I_{sat}$ with V_{bg}= 40 V at 70 K is 1.2%. This is predictable since both of MoS_2 and SiO_2 have a low thermal conductivity indicating a poor heat transport behavior[32,33]. The local heating of MoS_2-SiO_2 interfaces could be even more pronounced compared to that of Si-SiO_2 interfaces in modern SOI (silicon-on-insulator) structures, which could be an important issue for high-performance MoS_2 transistors with scaling[50]. For efficient heat dissipation from MoS_2 channel, substrates with high thermal conductivity (κ) are desirable, *e.g.*, Al_2O_3 (κ = 35 W/m·K), instead of commonly used SiO_2 (κ = 1.4 W/m·K)[33]. Figure 5b shows the output characteristic of the top-gate

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MoS_2 transistors at 70 K with top-gate biases V_{tg} range from 4 to 10 V with a 2 V step and V_{bg} fixed at 0 V. We didn't observe any NDR effect even 18% improvement in drain current over the sample in (a), indicating an efficient heat dissipation using high thermal conductivity Al_2O_3. With increasing V_{bg} to 40 V, the drain current is over 600 μA/μm without NDR effect as shown in Fig. 5c. When decreasing the temperature down to 4.3 K, the drain current increases accordingly as shown in Fig. 5d-f. The saturation current degradation $\Delta I/I_{sat}$ of the back-gate device with V_{bg} = 40 V at 4.3 K is 1.6% as shown in Figure 5d, which is larger than that of 1.2% at 70 K in (a). This confirms that the NDR effect is more pronounced in higher drain current due to self-heating effect[51]. At V_{bg} = 40 V and 4.3 K, the drain current of the top-gate device is larger than 620 μA/μm as shown in Figure 5f, up to 660 μA/μm at V_{tg} = 10 V. When the drain current is greater than 635 μA/μm, we observed the sign of NDR effect again. The $\Delta I/I_{sat}$ with V_{tg} = 10 V and V_{bg} = 40 V at 4.3 K is 0.5%, which is three times smaller than that in (d). This result shows that Al_2O_3/HfO_2 is more efficient to remove self-heating. It should be noted that the NDR is strongly related with the width and channel length of MoS_2 transistors, which determines the area of dissipation during device operation. With further scaling, the NDR phenomena is more easily observed due to the increased heat generation and reduced area for heat dissipation.

CONCLUSIONS

In conclusion, we report a high-performance MoS_2 transistor. We systematically compare the effect of Al_2O_3/HfO_2 and SiO_2 substrates on the mobility, drain current, oxide trap density, and NDR of MoS_2 devices. Benefiting from the high dielectric constant and high thermal conductivity of Al_2O_3/HfO_2, the MoS_2 transistor with Al_2O_3/HfO_2 exhibits a high mobility of 81 $cm^2/V\cdot s$ and less oxide trap density. The maximum drain current of the top-gate device with a 1 μm-channel-length is

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up to 660 μA/μm at 4.3 K. Meanwhile, Al_2O_3/HfO_2 substrate reduces the self-heating effect. Our work provides a viable path to improve the device performance of TMD-based FETs.

METHODS

By standard scotch-tape techniques, few-layer MoS_2 were transferred to heavily doped silicon substrate which was capped with 90 nm SiO_2. Then it soaked in undiluted 1, 2 dichloroethane (DCE) at room temperature for more than 12 h. Source/drain regions were defined by e-beam lithography, followed by a Ni/Au metallization of 15/45 nm with e-beam evaporator. The gap between source and drain was 1 μm. After the device was first measured with back gate only, the top gate dielectric was grown by ALD. First, a 25 nm Al_2O_3 was deposited with trimethylaluminum and H_2O as precursors at 75 ºC and then 20 nm HfO_2 was in situ deposited using tetradimethylaminohafnium and H_2O as precursors at 150 ºC. The dielectric constant of Al_2O_3 and HfO_2 are 6 and 12, respectively. The top gate was defined with e-beam lithography and Ti/Au of 15/45 nm was used as the top gate. No annealing was performed during the process.

FIGURES

Figure 1. (a) Cross-section schematic view of a back-gate MoS_2 device. (b) Cross-section schematic view of a dual-gate MoS_2 device. (c) AFM images of the MoS_2 device. The MoS_2 flake is 4.2 nm measured by AFM.

Figure 2. (a) Transfer characteristics of the back-gate MoS_2 device before and after Al_2O_3/HfO_2 capping at 300 K. Inset: The linear coordinated transfer curves. (b) Transfer characteristics of the back-gate and top-gate MoS_2 device at 300 K. (c) Output characteristics of the back-gate MoS_2 device at 300 K. V_{bg} is from -40 to 40 V in 5 V step with V_d from 0 to 3 V. (d) Output characteristics of the top-gate MoS_2 transistor with V_{bg} fixed at 0 V at 300 K. V_{tg} is from -16 to 10 V in 2 V step and V_d from 0 to 3 V. (e) Comparison of maximum drain current of the same two devices in (c) and (d) at different temperatures. (f) Comparison of g_m of the same two devices in (c) and (d) at various temperatures.

Figure 3. Output characteristics of the top-gate MoS_2 transistor at 300 K with 3 V steps in V_{tg} from -10 to 8 V with comparison between DC measurement and different pulse widths (pulse width = 5, 15, and 25 ms) for (a) V_{bg} = -30 V and (b) V_{bg} = 0 V. (c) ΔI_d as a function of V_{bg} for the same device in (a) at various V_{tg} with V_d = 2 V. (d) ΔI_d as a function of V_{tg} for the same device in (a) at various V_{bg} with V_d = 2 V.

Figure 4. (a) Inverse noise amplitude $1/A$ as a function of carrier density at V_d = 0.2 V. (b) Input gate voltage noise versus frequency for the same two devices in (a). (c) Oxide trap density versus trap depth, derived from the low-frequency noise spectrum at their corresponding threshold voltage $V_{th,t}$ and $V_{th,b}$.

Figure 5. (a) The output characteristics of the back-gate MoS_2 transistor at 70 K. V_{bg} is from 25 to 40 V with 5 V steps. The I_d-V_d characteristics of the top-gate device at 70 K with (b) V_{bg} = 0 V, and (c)

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V_{bg} = 40 V. V_{tg} is from 4 to 10 V with 2 V steps. (d-f) The I_d-V_d characteristics of the corresponding devices in (a-c) at 4.3 K.

ASSOCIATED CONTENT

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Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

This project was supported by the Natural Science Foundation of China (Grant Nos. 61574066, 11404118 and 61390504).

REFERENCES

(1) Wang, Q. H.; Kalantar-Zadeh, K.; Kis, A.; Coleman, J. N.; Strano, M. S. Electronics and Optoelectronics of Two-Dimensional Transition Metal Dichalcogenides. *Nat. Nanotechnol.* **2012,** *7* (11), 699-712.

(2) Butler, S. Z.; Hollen, S. M.; Cao, L.; Cui, Y.; Gupta, J. A.; Gutierrez, H. R.; Heinz, T. F.; Hong, S. S.; Huang, J.; Ismach, A. F. Progress, Challenges, and Opportunities in Two-Dimensional Materials Beyond Graphene. *ACS Nano* **2013,** *7* (4), 2898-2926.

(3) Chhowalla, M.; Shin, H. S.; Eda, G.; Li, L.-J.; Loh, K. P.; Zhang, H. The Chemistry of Two-Dimensional Layered Transition Metal Dichalcogenide Nanosheets. *Nat. Chem.* **2013,** *5* (4), 263-275.

(4) Jongho, L.; Hsiao-Yu, C.; Tae-Jun, H.; Huifeng, L.; Ruoff, R. S.; Dodabalapur, A.; Akinwande, D. In *High-Performance Flexible Nanoelectronics: 2D Atomic Channel Materials for Low-Power Digital and High-Frequency Analog Devices*, 2013 IEEE International Electron Devices Meeting (IEDM)., 9-11 Dec. 2013; pp 19.2.1-19.2.4.

(5) Koski, K. J.; Cui, Y. The New Skinny in Two-Dimensional Nanomaterials. *ACS Nano* **2013,** *7* (5), 3739-3743.

(6) Jariwala, D.; Sangwan, V. K.; Lauhon, L. J.; Marks, T. J.; Hersam, M. C. Emerging Device Applications for Semiconducting Two-Dimensional Transition Metal Dichalcogenides. *ACS Nano* **2014,** *8* (2), 1102-1120.

(7) Schwierz, F.; Pezoldt, J.; Granzner, R. Two-Dimensional Materials and Their Prospects in Transistor Electronics. *Nanoscale* **2015,** *7* (18), 8261-8283.

(8) Radisavljevic, B.; Radenovic, A.; Brivio, J.; Giacometti, V.; Kis, A. Single-Layer MoS_2 Transistors. *Nat. Nanotechnol.* **2011,** *6* (3), 147-150.

(9) Yoon, Y.; Ganapathi, K.; Salahuddin, S. How Good Can Monolayer MoS_2 Transistors Be? *Nano Lett.* **2011,** *11* (9), 3768-3773.

(10) Liu, H.; Neal, A. T.; Ye, P. D. Channel Length Scaling of MoS_2 MOSFETs. *ACS Nano* **2012,** *6* (10), 8563-8569.

(11) Du, Y.; Liu, H.; Neal, A. T.; Si, M.; Ye, P. D. Molecular Doping of Multilayer MoS Field-Effect Transistors: Reduction in Sheet and Contact Resistances. *IEEE Electron Devices Lett.* **2013,** *34* (10), 1328-1330.

(12) Li, X.; Yang, L.; Si, M.; Li, S.; Huang, M.; Ye, P.; Wu, Y. Performance Potential and Limit of MoS_2 Transistors. *Adv. Mater.* **2015,** *27* (9), 1547-1552.

(13) Yu, L.; Lee, Y.-H.; Ling, X.; Santos, E. J.; Shin, Y. C.; Lin, Y.; Dubey, M.; Kaxiras, E.; Kong, J.; Wang, H. Graphene-MoS_2 Hybrid Technology for Large-Scale Two-Dimensional Electronics. *Nano Lett.* **2014,** *14* (6), 3055-3063.

(14) Yang, L.; Majumdar, K.; Du, Y.; Liu, H.; Wu, H.; Hatzistergos, M.; Hung, P.; Tieckelmann, R.; Tsai, W.; Hobbs, C. High-Performance MoS_2 Field-Effect Transistors Enabled by Chloride Doping: Record Low Contact Resistance (0.5 kohm·µm) and Record High Drain Current (460 µA/µm). *Symposia on VLSI Technology and Circuits (VLSI 2014)* **2014**, 192-193.

(15) Krasnozhon, D.; Lembke, D.; Nyffeler, C.; Leblebici, Y.; Kis, A. MoS_2 Transistors Operating at Gigahertz Frequencies. *Nano Lett.* **2014,** *14* (10), 5905-5911.

(16) Late, D. J.; Huang, Y.-K.; Liu, B.; Acharya, J.; Shirodkar, S. N.; Luo, J.; Yan, A.; Charles, D.; Waghmare, U. V.; Dravid, V. P. Sensing Behavior of Atomically Thin-Layered MoS_2 Transistors. *ACS Nano* **2013,** *7* (6), 4879-4891.

(17) Mak, K. F.; Lee, C.; Hone, J.; Shan, J.; Heinz, T. F. Atomically Thin MoS_2: A New Direct-Gap Semiconductor. *Phys. Rev. Lett.* **2010,** *105* (13), 136805.

(18) Lee, Y. H.; Zhang, X. Q.; Zhang, W.; Chang, M. T.; Lin, C. T.; Chang, K. D.; Yu, Y. C.; Wang, J. T. W.; Chang, C. S.; Li, L. J. Synthesis of Large-Area MoS_2 Atomic Layers with Chemical Vapor Deposition. *Adv. Mater.* **2012,** *24* (17), 2320-2325.

(19) Wang, H.; Yu, L.; Lee, Y.; Fang, W.; Hsu, A.; Herring, P.; Chin, M.; Dubey, M.; Li, L.; Kong, J.; Palacios, T. In *Large-Scale 2D Electronics Based on Single-Layer MoS_2 Grown by Chemical Vapor Deposition*, 2012 IEEE International Electron Devices Meeting (IEDM), , 10-13 Dec. 2012; pp 4.6.1-4.6.4.

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60

(20) Zhu, W.; Low, T.; Lee, Y.-H.; Wang, H.; Farmer, D. B.; Kong, J.; Xia, F.; Avouris, P. Electronic Transport and Device Prospects of Monolayer Molybdenum Disulphide Grown by Chemical Vapour Deposition. *Nat. Commun.* **2014,** *5*, 3087-3094.

(21) Kang, K.; Xie, S.; Huang, L.; Han, Y.; Huang, P. Y.; Mak, K. F.; Kim, C.-J.; Muller, D.; Park, J. High-Mobility Three-Atom-Thick Semiconducting Films with Wafer-Scale Homogeneity. *Nature* **2015,** *520* (7549), 656-660.

(22) Kaasbjerg, K.; Thygesen, K. S.; Jacobsen, K. W. Phonon-Limited Mobility in n-Type Single-Layer MoS_2 from First Principles. *Phys. Rev. B* **2012,** *85* (11), 115317.

(23) Jena, D.; Konar, A. Enhancement of Carrier Mobility in Semiconductor Nanostructures by Dielectric Engineering. *Phys. Rev. Lett.* **2007,** *98* (13), 136805.

(24) Bao, W.; Cai, X.; Kim, D.; Sridhara, K.; Fuhrer, M. S. High Mobility Ambipolar MoS_2 Field-Effect Transistors: Substrate and Dielectric Effects. *Appl. Phys. Lett.* **2013,** *102* (4), 042104.

(25) Cui, X.; Lee, G.-H.; Kim, Y. D.; Arefe, G.; Huang, P. Y.; Lee, C.-H.; Chenet, D. A.; Zhang, X.; Wang, L.; Ye, F.; Pizzocchero, F.; Jessen, B. S.; Watanabe, K.; Taniguchi, T.; Muller, D. A.; Low, T.; Kim, P.; Hone, J. Multi-Terminal Transport Measurements of MoS_2 using a Van Der Waals Heterostructure Device Platform. *Nat. Nanotechnol*. **2015**, 10 (6), 534-540.

(26) Zhou, C.; Wang, X.; Raju, S.; Lin, Z.; Villaroman, D.; Huang, B.; Chan, H.; Chan, Mansun.; Chai, Y.; Low Voltage and High ON/OFF Ratio Field-Effect Transistors Based on CVD MoS_2 and Ultra High-k Gate Dielectric PZT. *Nanoscale*, **2015**, 7 (19), 8695.

(27) Xu, K.; Wang, Y.; Zhao, Y.; Chai, Y.; Modulation Doping of Transition Metal Dichalcogenide/Oxide Heterostructures. *J. Mater. Chem. C*, **2017**, 5 (2), 376-381.

(28) Zhou, C.; Zhao,Y.; Raju, S.; Wang, Y.; Lin, Z.; Chan, Mansun.; Chai, Yang.; Carrier Type Control of WSe_2 Field-Effect Transistor by Thickness Modulation and MoO_3 Layer Doping. *Adv. Funct. Mater.* **2016**, 26 (23), 4223-4230.

(29) Ganapathi, K.; Bhattacharjee, S.; Mohan, S.; Bhat, N.; High-Performance HfO_2 Back Gated Multilayer MoS_2 Transistors, *IEEE Electron Device Lett*. **2016**, 37 (6), 797-800.

(30) Wen, M.; Xu, J.; Liu, L.; Lai, P.; Tang, W.; Improved Electrical Performance of Multilayer MoS_2 Transistor with NH_3-Annealed ALD HfTiO Gate Dielectric. *IEEE Trans. on Electron Devices*, **2017**, 64 (3), 1020-1025.

(31) Yu, Z.; Ong, Z.; Pan, Y.; Cui, Y.; Xin, R.; Shi, Yi.; Wang, B.; Wu, Y.; Chen, T.; Zhang, Y.; Zhang, G.; Wang, X.; Realization of Room-Temperature Phonon-Limited Carrier Transport in Monolayer MoS_2 by Dielectric and Carrier Screening. *Adv. Mater.,* **2016**, 28 (3), 547–552.

(32) Schwierz, F. In *Transition Metal Dichalcogenides—A New Material Class for Semiconductor Electronics?*, 2013 IEEE 10th International Conference on ASIC (ASICON),, IEEE: 2013; pp 1-4.

(33) Yum, J.; Bersuker, G.; Oh, J.; Banerjee, S. Theoretical Approach to Evaluating Beryllium Oxide as a Gate Dielectric Considering Electromagnetics and Thermal Stability. *Appl. Phys. Lett.* **2012,** *100* (5), 053501.

(34) Young, C. D.; Zhao, Y.; Heh, D.; Choi, R.; Lee, B. H.; Bersuker, G. Pulsed I_d-V_g Methodology and Its Application to Electron-Trapping Characterization and Defect Density Profiling. *IEEE Trans. on Electron Devices,* **2009,** 56, (6), 1322-1329.

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(35) Young, C. D.; Zhao, Y.; Pendley, M.; Lee, B. H.; Matthews, K.; Sim, J. H.; Choi, R.; Brown, G. A.; Murto, R. W.; Bersuker, G. Ultra-Short Pulse Current-Voltage Characterization of the Intrinsic Characteristics of High-κ Devices. *Jpn. J. Appl. Phys.* **2005,** *44* (4S), 2437.

(36) Young, C. D.; Heh, D.; Choi, R.; Lee, B. H.; Bersuker, G. The Pulsed I_d-V_g Methodology and Its Application to the Electron Trapping Characterization of High-κ gate Dielectrics. *J. Semi. Technol. Sci.* **2010,** *10* (2), 79-99.

(37) Razavi, B. A Study of Phase Noise in CMOS Oscillators. *IEEE J. Solid-St. Circ.* **1996,** *31* (3), 331-343.

(38) Von Haartman, M.; Östling, M. *Low-Frequency Noise in Advanced MOS Devices*, Springer Science & Business Media: 2007.

(39) Vandamme, L.; Li, X.; Rigaud, D. *1/f Noise in MOS Devices, Mobility or Number Fluctuations? IEEE Trans. on Electron Devices,* **1994,** 41 (11), 1936-1945.

(40) Hooge, F. *1/f Noise Sources. IEEE Trans. on Electron Devices,* **1994,** 41 (11), 1926-1935.

(41) Xu, G.; Torres Jr, C. M.; Zhang, Y.; Liu, F.; Song, E. B.; Wang, M.; Zhou, Y.; Zeng, C.; Wang, K. L. Effect of Spatial Charge Inhomogeneity on 1/*f* Noise Behavior in Graphene. *Nano Lett.* **2010,** *10* (9), 3312-3317.

(42) Renteria, J.; Samnakay, R.; Rumyantsev, S. L.; Jiang, C.; Goli, P.; Shur, M. S.; Balandin, A. A. Low-Frequency 1/*f* Noise in MoS_2 Transistors: Relative Contributions of the Channel and Contacts. *Appl. Phys. Lett.* **2014,** *104* (15), 153104-153108.

(43) Kwon, H.-J.; Kang, H.; Jang, J.; Kim, S.; Grigoropoulos, C. P. Analysis of Flicker Noise in Two-Dimensional Multilayer MoS_2 Transistors. *Appl. Phys. Lett.* **2014,** *104* (8), 083110.

(44) Vandamme, L. K.; Hooge, F. What Do We Certainly Know About Noise in MOSTs? *IEEE Trans. on Electron Devices,* **2008,** *55* (11), 3070-3085.

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(45) Scarpino, M.; Gupta, S.; Lin, D.; Alian, A.; Crupi, F.; Collaert, N.; Thean, A.; Simoen, E. Border Traps in InGaAs nMOSFETs Assessed by Low-Frequency Noise. *IEEE Electron Device Lett.* **2014,** *35* (7), 720-722.

(46) Wang, B. C.; Lu, Y. Y.; Chang, S. J.; Chen, J. F.; Tsai, S. C.; Hsu, C. H.; Yang, C. W.; Chen, C. G.; Cheng, O.; Huang, P. C. Comparison of the Trap Behavior between ZrO_2 and HfO_2 Gate Stack nMOSFETs by $1/f$ Noise and Random Telegraph Noise. *IEEE Electron Device Lett.,* **2013,** *34* (2), 151-153.

(47) Na, J.; Joo, M.; Shin, M.; Huh, J.; Kim, J.; Piao, M.; Jin, J.; Jang, H.; Choi, H.; Shim, J.; Kim, G. Low-Frequency Noise in Multilayer MoS_2 Field-Effect Transistors: the Effect of High-k Passivation. *Nanoscale*. **2014**, 6 (1), 433-441.

(48) Li, Tao.; Wan, B.; Du, G.; Zhang, B.; Zeng, Z. Electrical Performance of Multilayer MoS_2 Transistors on High-k Al_2O_3 Coated Si Substrates. *AIP Adv*. **2015**, 5 (5), 057102.

(49) Anghel, C.; Gillon, R.; Ionescu, A. M. Self-heating Characterization and Extraction Method for Thermal Resistance and Capacitance in HV MOSFETs. *IEEE Electron Device Lett.,* **2004,** *25* (3), 141-143.

(50) Eilam, Y.; Connor, J.; Kirby, K.; Miguel, M.; Runjie, L.; Saurabh, V. ; Alex, J.; Christopher, M.; Feng, X.; Amir, B.; Eric, P. Energy Dissipation in Monolayer MoS_2 Electronics. *Nano Lett.* **2017**, 17 (6), 3429–3433.

(51) Islam, S.; Li, Z.; Dorgan, V. E.; Bae, M.-H.; Pop, E. Role of Joule Heating on Current Saturation and Transient Behavior of Graphene Transistors. *IEEE Electron Device Lett.* **2013,** *34* (2), 166-168.

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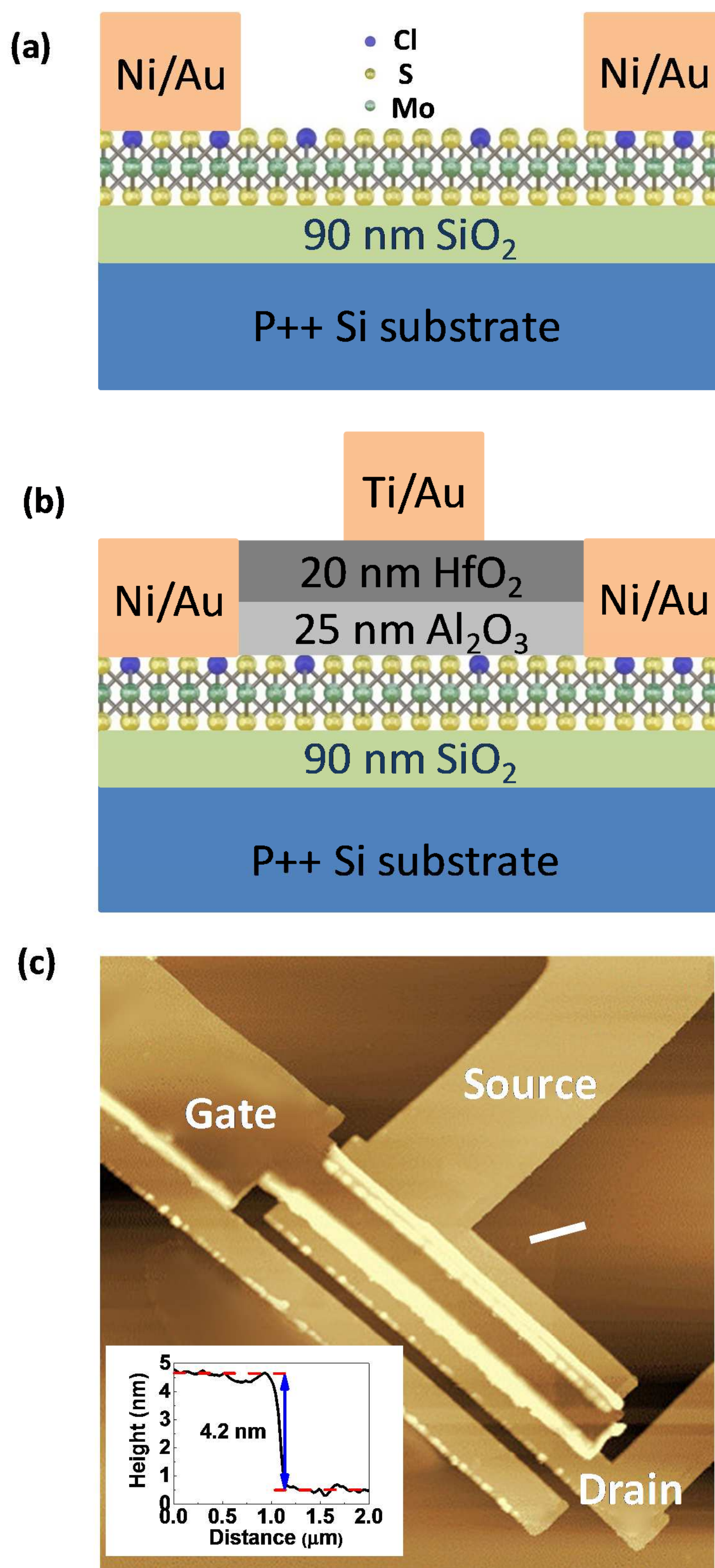

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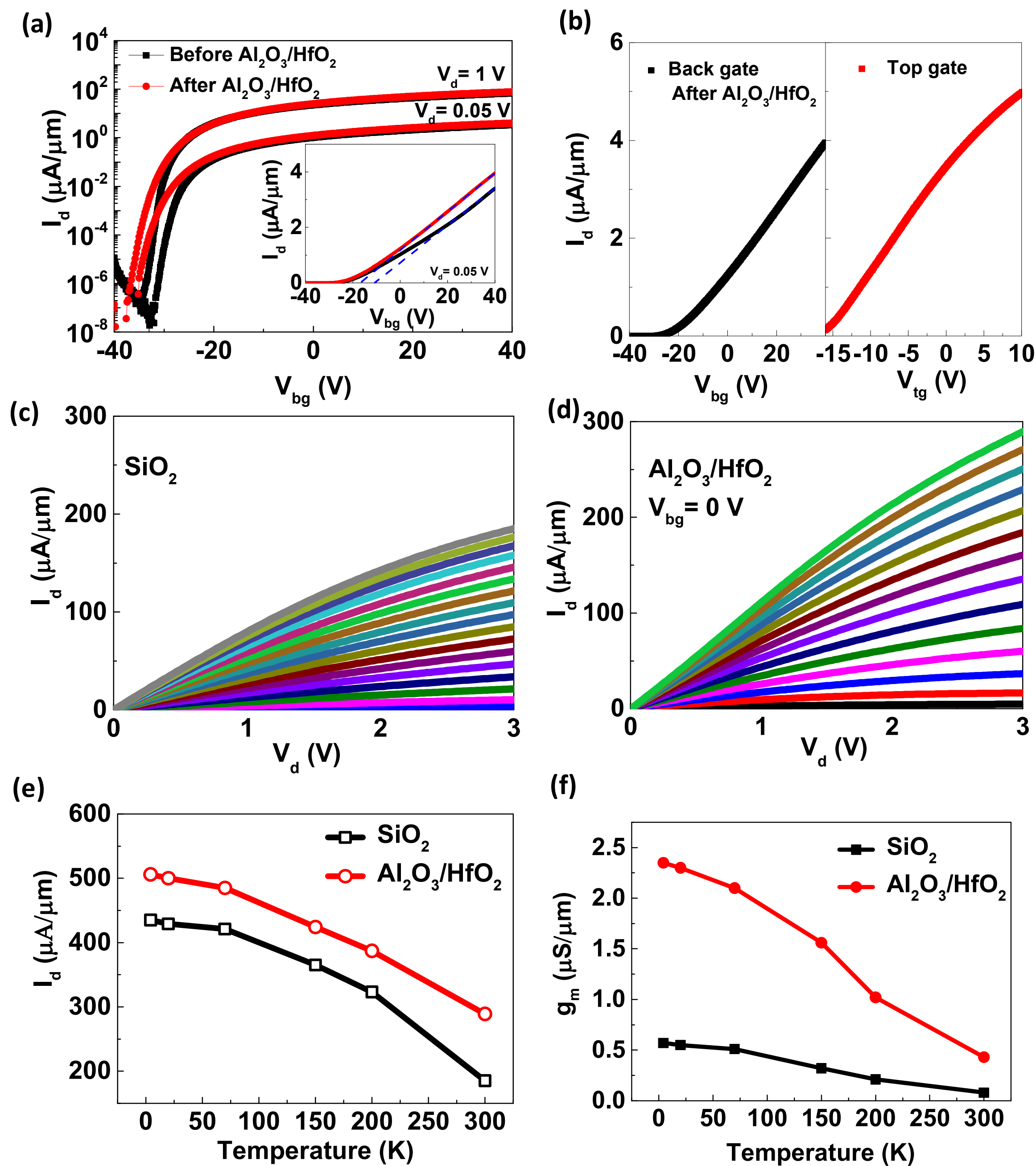
Figure 2



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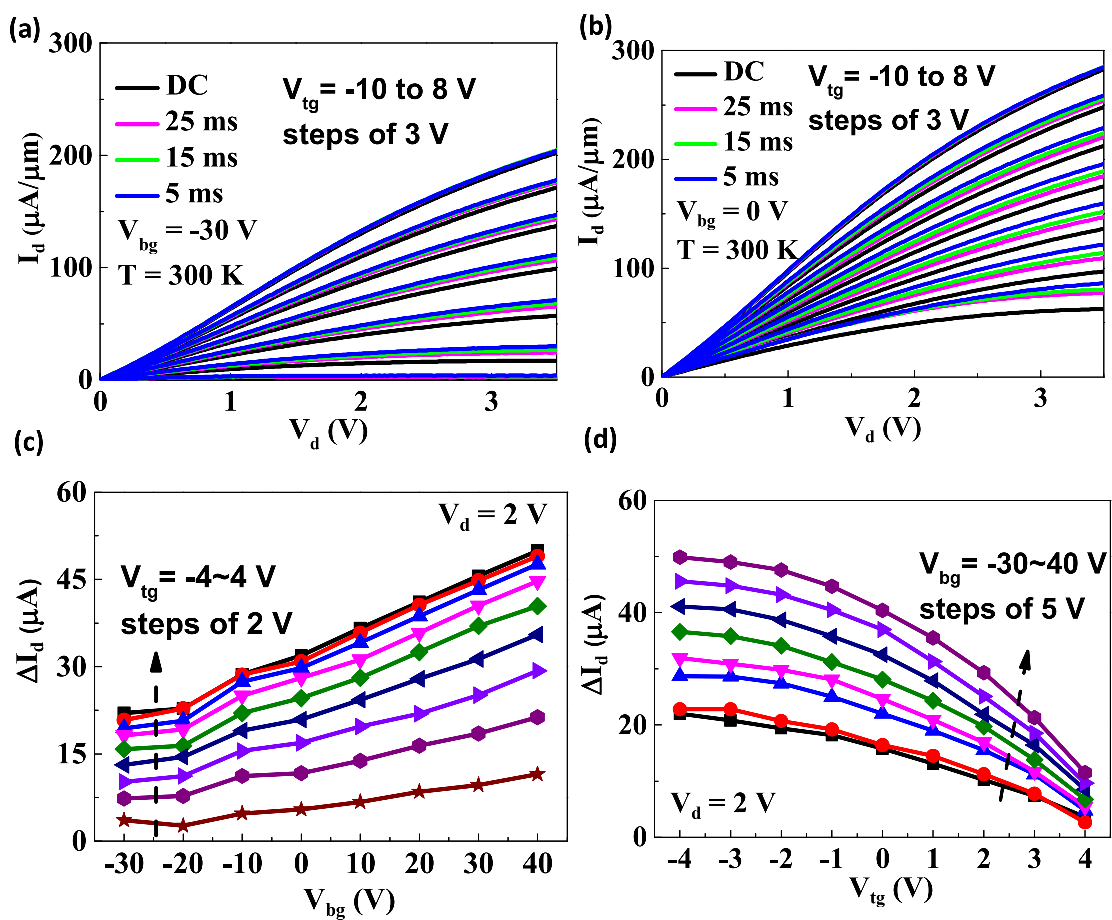

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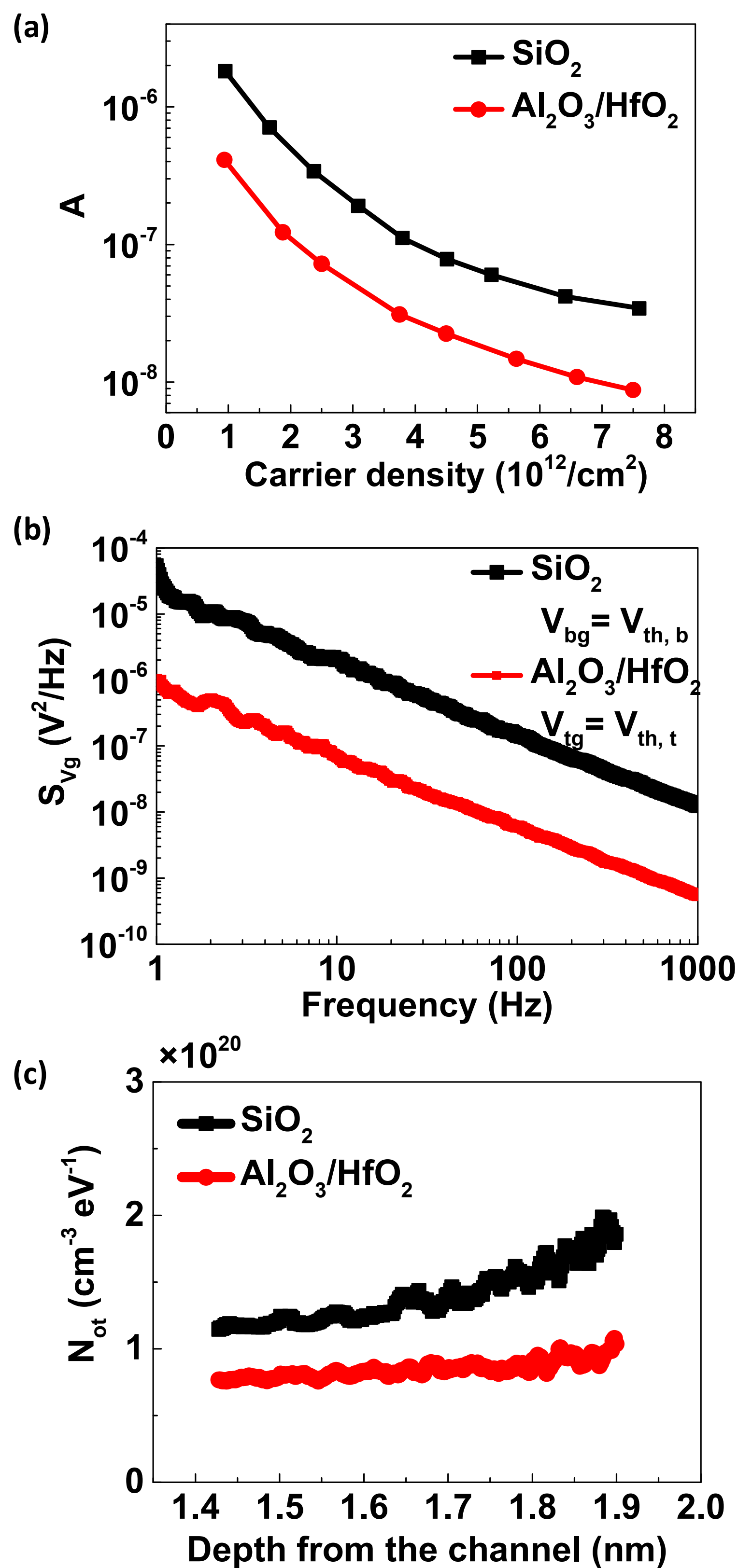

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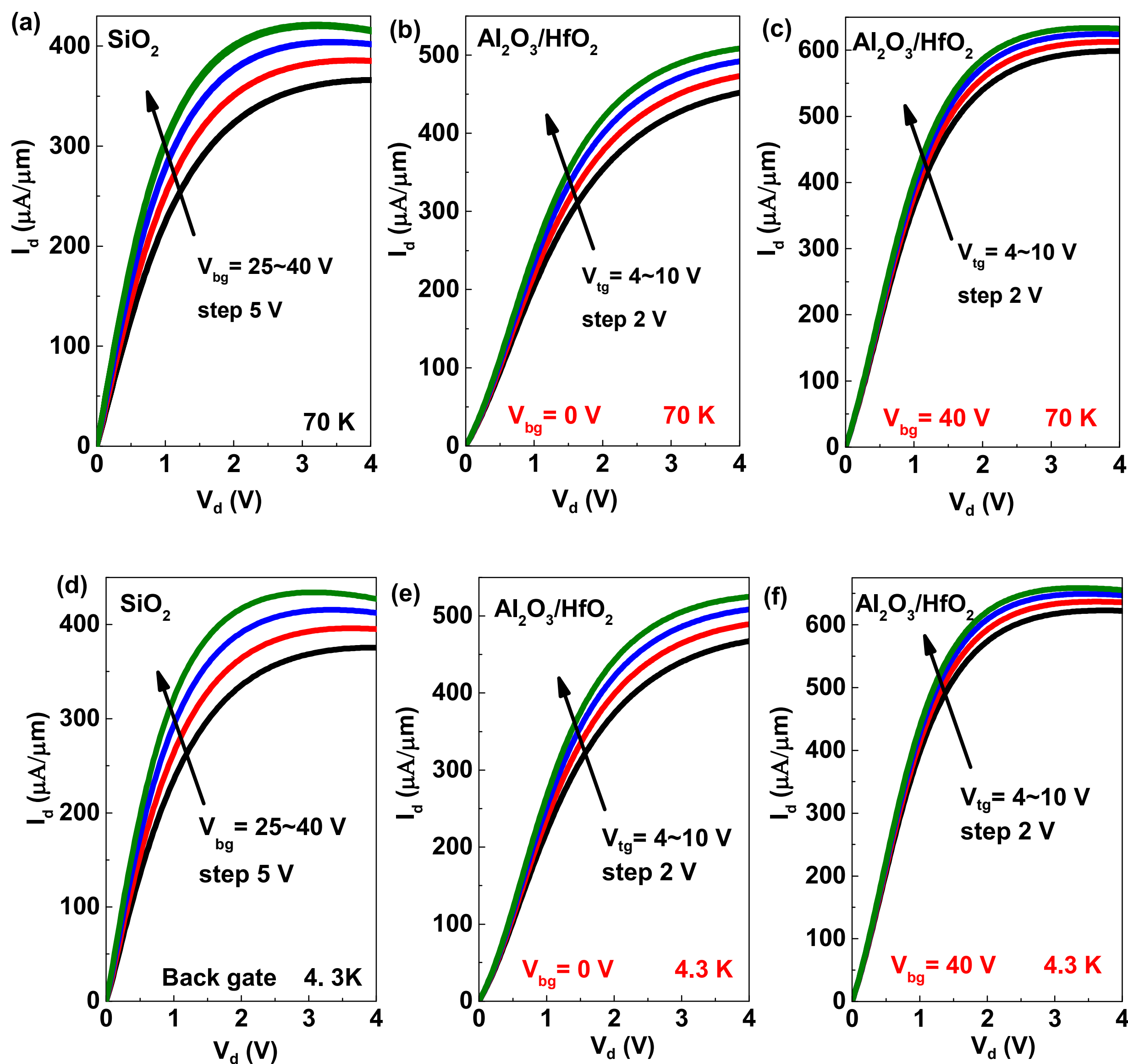
Figure 5



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