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Reconfigurable Logic-in-Memory and Multilingual Artificial Synapses Based on 2D Heterostructures

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Nonvolatile logic devices have attracted intensive research attentions recently for energy efficiency computing, where data computing and storage can be realized in the same device structure. Various approaches have been adopted to build such devices; however, the functionality and versatility are still very limited. Here, 2D van der Waals heterostructures based on direct bandgap materials black phosphorus and rhenium disulfide for the nonvolatile ternary logic operations is demonstrated for the first time with the ultrathin oxide layer from the black phosphorus serving as the charge trapping as well as band-to-band tunneling layer. Furthermore, an artificial electronic synapse based on this heterostructure is demonstrated to mimic trilingual synaptic response by changing the input base voltage. Besides, artificial neural network simulation based on the electronic synaptic arrays using the handwritten digits data sets demonstrates a high recognition accuracy of 91.3%. This work provides a path toward realizing multifunctional nonvolatile logic-in-memory applications based on novel 2D heterostructures.

1. Introduction

Computing-in-memory architecture is considered as one of the most promising beyond traditional complementary metal-oxide-semiconductor (CMOS) technology. The conventional von Neumann computing architecture faces a great challenge to provide higher performance and lower power consumption due to the bottleneck between the logic and memory blocks.[1–4] As a result, in-memory computing devices such as artificial synaptic devices and ternary content-addressable memory (TCAM) based on nonvolatile devices are promising candidates for future electronics and have drawn great research attention recently.[2,4–9] So far, many kinds of nonvolatile devices have been employed in experimental demonstrations, including resistive random access memory (RRAM),[10,11] phase-change memory (PCM),[12,13] ferroelectric field-effect transistor (FeFET),[14] and magnetic random access memory (MRAM).[15] Novel switching based on new channel materials is actively explored beyond these materials, particularly based on emerging 2D materials and their heterostructures.

Due to the diversity of energy band configurations, 2D van der Waals heterostructure has great potential to form multifunctional devices including memories and logic devices.[16–25] Recently, a high program/erase ratio of ≈10^9 nonvolatile memory was realized by stacking graphene/h-BN/MoS_2/$MoTe_2$.[26] In addition, quasi-nonvolatile applications[25] or programmable p–n junctions[27] with improved memory performance have also been created by using semi-floating gate technology. A high-performance tunable binary and ternary logic devices with a high gain of ≈152 based on BP/MoS_2 van der Waals heterostructures have been demonstrated.[21] Moreover, artificial synaptic devices based on 2D materials have also been demonstrated with the potential for versatile artificial neural networks (ANN) and neuromorphic computing.[6,28–32] However, the multifunctionality or versatility is still lacking in previously demonstrated devices regarding nonvolatile multi-valued logic operations and multilingual synaptic operations. In this work, we demonstrate the multifunctional black phosphorus (BP)[33–35] and rhenium disulfide (ReS_2)[36,37] van der Waals heterostructures for nonconventional logic and memory applications. The natural oxidation of BP forms a thin phosphorus oxide (PO_x) layer, which plays a role as the key functional charge-trapping layer.[31,32] In the first part of this work, a nonvolatile ternary logic inverter based on BP/ReS_2 heterostructure is demonstrated where the logic states "1," "1/2," and "0" can be modulated gradually by the input voltage pulses, forming a nonconventional logic output. Finally, a heterojunction-based artificial synapse with a trilingual response is demonstrated where reconfigurable synaptic effects are realized between the excitatory and inhibitory states. A handwritten digits recognition neural network simulation is implemented using the synaptic devices arrays based on the fact that the heterojunction

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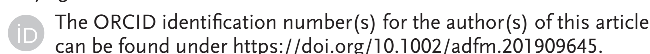
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artificial synapse exhibits repeatable and stable response of long-term plasticity characteristics. This demonstration of non-conventional logic and memory operations based on van der Waals heterostructures provides new insights and potential for next-generation non-von Neumann computing schemes.

2. Results and Discussion

2.1. Device Structure and Characterization

Figure 1a shows a schematic view of the BP/ReS_2 heterostructure device. The flakes of BP and ReS_2 were mechanically exfoliated and transferred together onto a 25 nm HfO_2-covered silicon substrates. The source and drain regions were patterned by electron-beam lithography (EBL) followed by electron-beam-evaporated 20/60 nm Ni/Au. The natural oxidation of the BP was carried out with 1 h exposure time in the cleanroom atmosphere after device fabrication. The high-resolution transmission electron microscope (TEM) image of the cross-section of BP/ReS_2 heterostructures is shown in Figure 1b where the highly crystalline layered lattice of BP and ReS_2 can be seen with 4 nm PO_x layer between BP and ReS_2. Figure 1c shows the device morphology where BP and ReS_2 flakes are marked with blue and red dotted lines, respectively. The thickness of the BP and the ReS_2 films determined by atomic force microscope (AFM) are about 10 and 7 nm, as shown in Figure S1, Supporting Information. The Raman spectra for three positions of the BP/ReS_2 heterostructures, including BP region, ReS_2 region, and the junction region, are shown in Figure 1d. Three characteristic peaks of BP at 362, 439, and 468 cm^{-1} correspond to $A^1{}_g$, B_{2g}, and $A^2{}_g$ modes, respectively. The E_{2g} peak at 152 cm^{-1}, A_{1g} peak at 212 cm^{-1} of ReS_2 can also be observed. Moreover, the Raman spectrum of the junction region is the superposition of the characteristic peaks of two materials, consistent with previous results.[18,38,39] Figure 1e,f shows the drain current I_d mapping of the BP/ReS_2 heterostructures as a function of drain and gate voltage at 300 K (Figure 1e) and 4.3 K (Figure 1f). The drain voltage is applied on BP terminal from −3 to 3 V and the ReS_2 source terminal is always grounded. Due to the different band alignment conditions under various voltage biases, the drain current exhibits non-monotonic dependence and continuous tunability with V_g from −4 to 4 V and V_d from −3 to 3 V, which is more distinctive at 4.3 K. These can be attributed to the band alignment movement where the junction changes from ReS_2-dominated n–p junction to BP-dominated n–p junction and n–n junction.

2.2. The Nonvolatile Ternary Logic Circuit

Multivalued logic devices can achieve greater data densities with a smaller footprint than conventional binary logic. Ternary logic circuit based on 2D materials has been realized by using the BP/ReS_2 heterostructure FET and a BP FET in series.[18,21,40] **Figure 2**a shows the individual transfer characteristic curves of BP transistor and BP/ReS_2 heterostructure transistor at a drain voltage of 1 V. The negative transconductance region of the

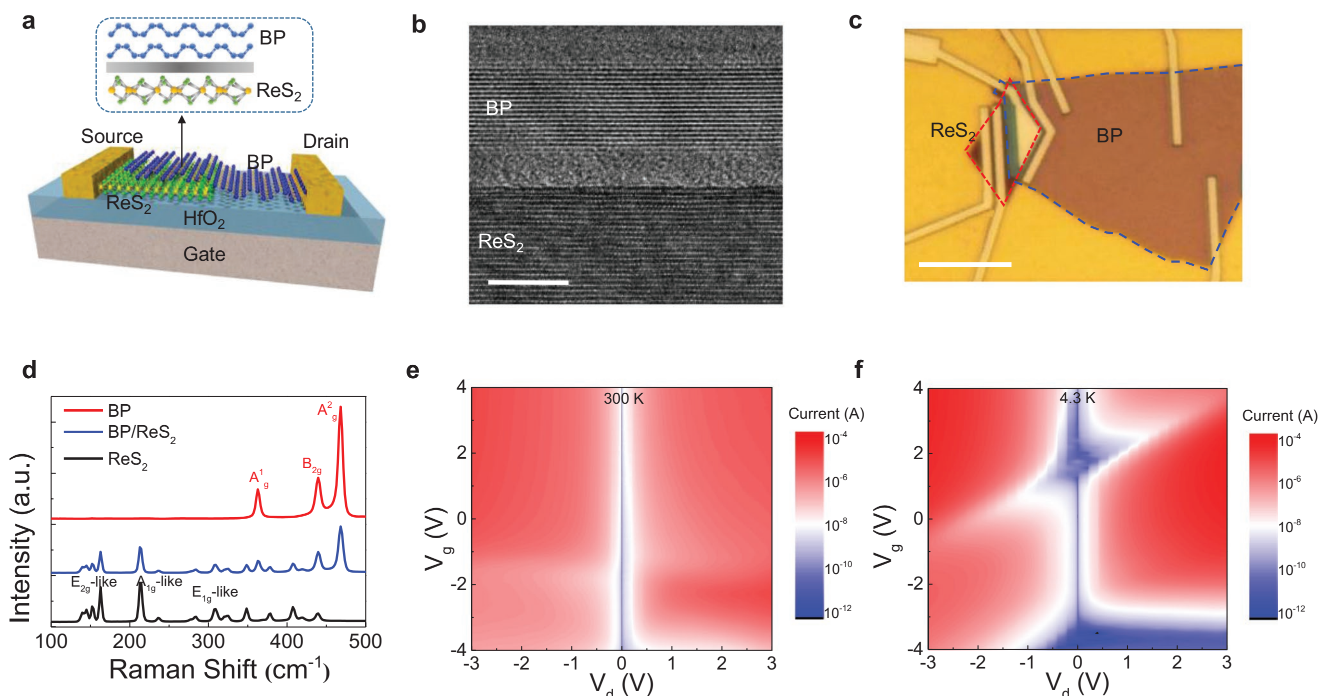

Figure 1. The van der Waals heterostructure and devices characterization. a) Schematic illustration of the BP/ReS_2 heterostructure devices and the schematic lattice cross-section of the junction interface. The drain electrode is deposited on the BP layer and the source is on ReS_2 layer. b) Cross-section high-resolution TEM image of BP/ReS_2 interfaces. A PO_x layer about ≈4 nm can be observed. The scale bar is 10 nm. c) Device morphology of the optical microscope. Scale bar: 10 µm. d) Raman spectra of BP, BP/ReS_2-overlapped, and ReS_2 regions, respectively. The current of the BP/ReS_2 junction with different V_d and V_g bias at e) 300 K and f) 4.3 K.

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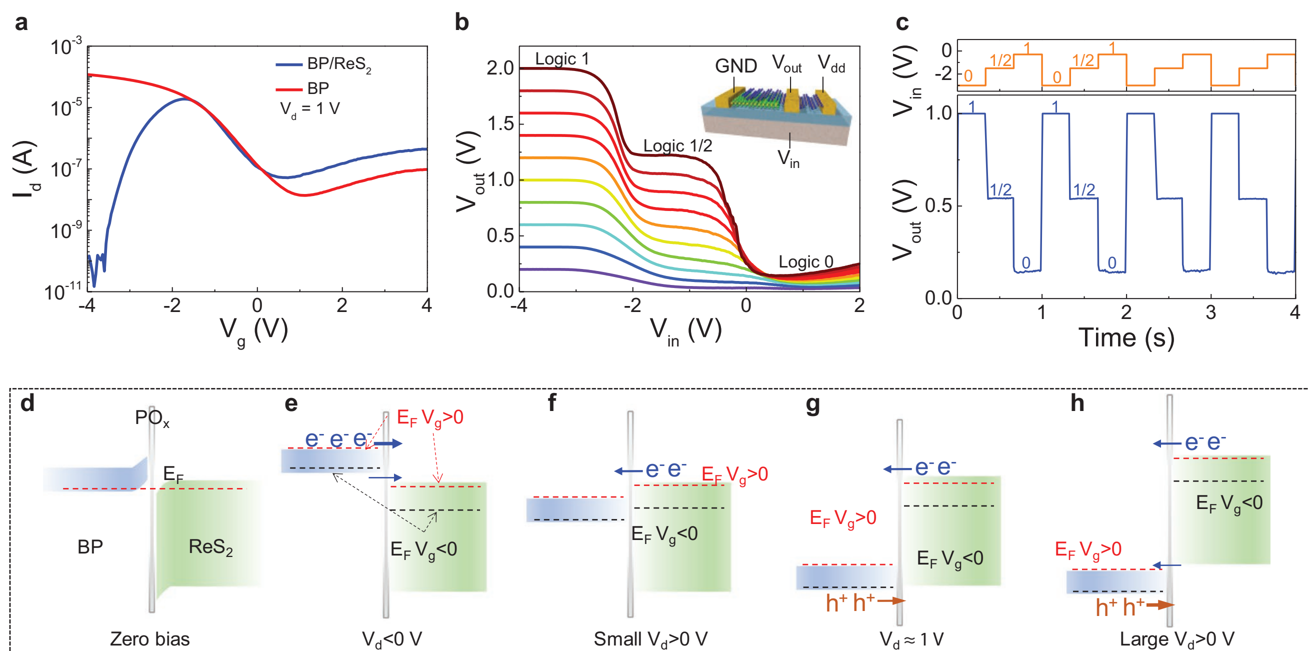

Figure 2. Ternary logic circuit. a) Transfer characteristics of the BP FET and BP/ReS_2 heterostructure FET at V_d = 1 V. b) V_{out} versus V_{in} for ternary inverters based on BP/ReS_2 heterostructure in-series BP FETs with V_{dd} from 0.1 to 2 V. Inset: schematic diagram of the ternary inverter circuit. c) The ternary logic output waveform of the inverter versus a ternary input waveform at 1 Hz. d) The energy band diagram of the heterostructure in the thermal equilibrium state with zero bias. e) The energy band diagram of the heterostructure with negative V_d bias and f–h) positive V_d bias.

heterostructure arises from the band-to-band tunneling mechanism where drain bias pulls the energy band of the BP down and forms a high tunneling efficiency region. The dominant current will then change from the ReS_2 n-type transport to the n-type hole tunneling through the heterojunction, which shows a decreasing trend as the gate bias increases. Beyond the negative transconductance region, the current will rise again due to the strong n–n junction as the gate bias further increases. The ternary inverter of V_{out} versus V_{in} with V_{dd} from 0.2 to 2 V is plotted in Figure 2b, where the device schematic of the ternary inverter is shown in the inset. The output characteristics show three distinct logic state regions including "logic 1" with the input voltage $V_{in} < -2$ V, "logic 1/2" when $-2 \text{ V} < V_{in} < 0$ V, and "logic 0" with the input voltage $V_{in} > 0$ V. The additional middle logic (logic 1/2) comes from the region with strong band-to-band tunneling where the BP transistor and BP/ReS_2 heterostructure transistor have almost identical current trends at $-2 \text{ V} < V_g < 0$ V as shown in Figure 2a. The dynamic output characteristics of the ternary logic inverter triggered by the three-level input voltage pulses are presented in Figure 2c where the middle logic is clearly visible in addition to the original two states. The energy band diagrams of the heterostructure with various voltage biases are plotted in Figure 2d–h. Figure 2d shows the energy band diagram of BP/PO_x/ReS_2 in the thermal equilibrium state with zero biases. The doping level of the lateral heterostructure is controlled by V_g. Under negative V_d bias (Figure 2e), the energy band of the BP will be pulled up and the energy band configuration of the heterostructure is type III. The overall transport mechanism of the device is based on diffusion and tunneling. Figure 2f–h shows the type-I to type-III band alignments of the heterostructure with the positive V_d pulled down the energy band of BP, creating the ternary logic function as discussed before.

Furthermore, the native oxidation of the BP layer forms a charge-trapping layer on the surface, behaving as a charge reserve layer as shown in **Figure 3**a. As a result, the voltage transfer curves of the ternary inverter also show a significant hysteresis under double voltage sweep as presented in Figure 3b. It can be seen that the two separate output states can be obtained depending on the voltage sweep directions at $V_{in} = -1.8$ V showing "1/2" and "1" and at $V_{in} = 0.3$ V showing "0" and "1/2", marked by the dashed line. The "1/2" and "1" two-level output can be better viewed in the output characteristics with pulsed V_{in} at a fixed $V_{in_base} = -1.8$ V as shown in Figure 3c. When the pulse width decreases from 50 to 1 ms, the "logic 1" shows little changes but "logic 1/2" output voltage increases accordingly. Similarly, the "0" and "1/2" two-level output can also be switched by pulsed V_{in} at a fixed $V_{in_base} = 0.3$ V. The "logic 0" shows little changes but "1/2" output voltage increases with decreasing pulse width as shown in Figure 3d. The results of the pulse switching show that the nonvolatile ternary inverter can work with a variety of input conditions.

2.3. Artificial Electric Trilingual Synapse

Artificial synapses can be used for ANNs and neuromorphic computing, which holds great potential for next-generation computing architecture with low energy consumption.[7,12] A schematic diagram of biological and artificial electronic synapses is shown in **Figure 4**a. The gate terminal acts as the presynaptic input terminal while the source terminal acts as

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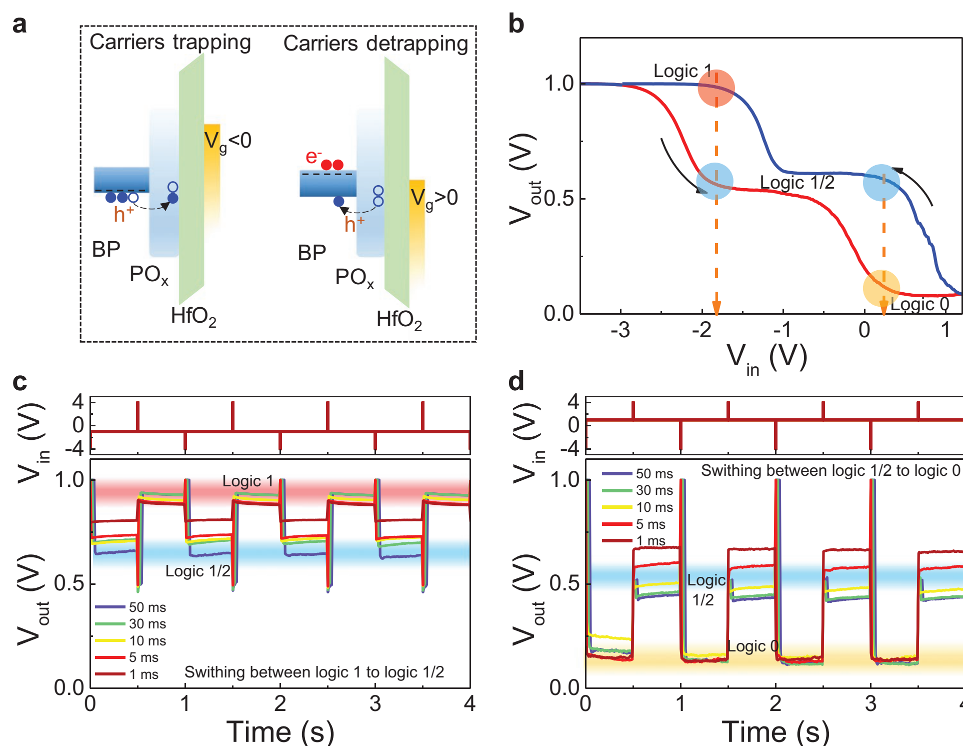

Figure 3. Nonvolatile ternary logic circuit. a) Schematic band diagrams for carriers trapping and de-trapping processes under negative V_g bias and positive V_g bias conditions. b) Typical double swept voltage transfer characteristics of a ternary logic inverter with V_{dd} = 1 V. c) The output switching between logic 1/2 to logic 1 at different V_{in} pulse width with a fixed V_{in} pulse amplitude of ±4 V and V_{in_base} = –1.8 V. d) The output switching between logic 0 and logic 1/2 at different V_{in} pulse width at V_{in_base} = 0.3 V.

postsynaptic output. Figure 4b shows the synaptic behavior under three electrostatic V_g bias conditions with a V_g pulse amplitude of 4 V. The postsynaptic current (PSC) shows both long-term excitatory and long-term inhibitory responses by tuning the base of the bias voltage of V_g (2, 0, –2 V) at a fixed V_d = 1 V. The drain current map as the function of V_d and double swept V_g was plotted, corresponding to the different synaptic behavior as shown in Figure 4c. As we discussed before, a positive input pulse will inject the electron to PO_x layer, resulting in an increase in the PSC at V_{g_base} = 0 V and a decrease in the PSC at V_{g_base} = +2/–2 V. The weight change referring to the strength of the excitatory and inhibitory synaptic responses is defined as ΔPSC over the initial PSC. As shown in the device synaptic behavior dependence on V_{g_base} in Figure 4d, three regions emerge from inhibitory to excitatory and back to inhibitory response with the presynaptic input base voltage from –3 to 3 V, showing a trilingual response property as well as tunable weight changes at the same pulse amplitude of 4 V with V_d = 1 V. The unique tunability of trilingual response originates from the anti-ambipolar of the BP/ReS_2 heterostructure devices similar to the previous ternary inverter operation, which can be also extended to other TMD materials.[41,42] Figure 4e shows the weight change of the excitatory PSC as a function of the presynaptic input pulse with the amplitude of 4 V and base of 0 V. As the presynaptic input pulse width increases from 1µs to 100 ms, the weight change shows a monotonous increase trend from 5% up to over ≈10^4% as more and more carriers being captured into the PO_x trapping layer, resulting in a stronger effect for Fermi level movement. The largest long-term synaptic weight change reaches 23 300%, exceeding the previously reported results.[43,44] Continuous pulse stimulations are applied to the device to mimic the long-term potentiation (LTP) and depression (LTD) of synapses, which are essential synaptic functions for neuromorphic computing. Figure 4f shows the PSC by alternating 50 positive (4 V, 100 µs) and 50 negative (–4 V, 10 µs) input gate voltage pulses, exhibiting repeatable and stable response of long-term potentiation and long-term depression of biological synapse. The experimental results of long-term plasticity characteristics can be used to perform the ANNs with supervised learning by backpropagation. A fully-connected network with one hidden layer has been simulated using CrossSim platform.[7,45] The schematic view of the neural network for handwritten digits from Modified National Institute of Standards and Technology dataset is shown in Figure 4g with 784 input neurons, 300 hidden neurons, and 10 output neurons for 28 × 28 input pixels and 10 output classifications. The nonvolatile heterostructure devices were used as storage of the weight in the network and the change of the conductance of the artificial synapses was adopted as the weight update in the process of the backpropagation algorithm. It is worth noting that the synaptic weights of the network allow for efficient parallel update compared with CMOS architecture. In addition, another network with a size of 64 × 36 × 10 was trained using another datasets of small digits with 8 × 8 pixels from the "Optical Recognition of Handwritten Digits" dataset. The test recognition accuracies of the simulation with two datasets

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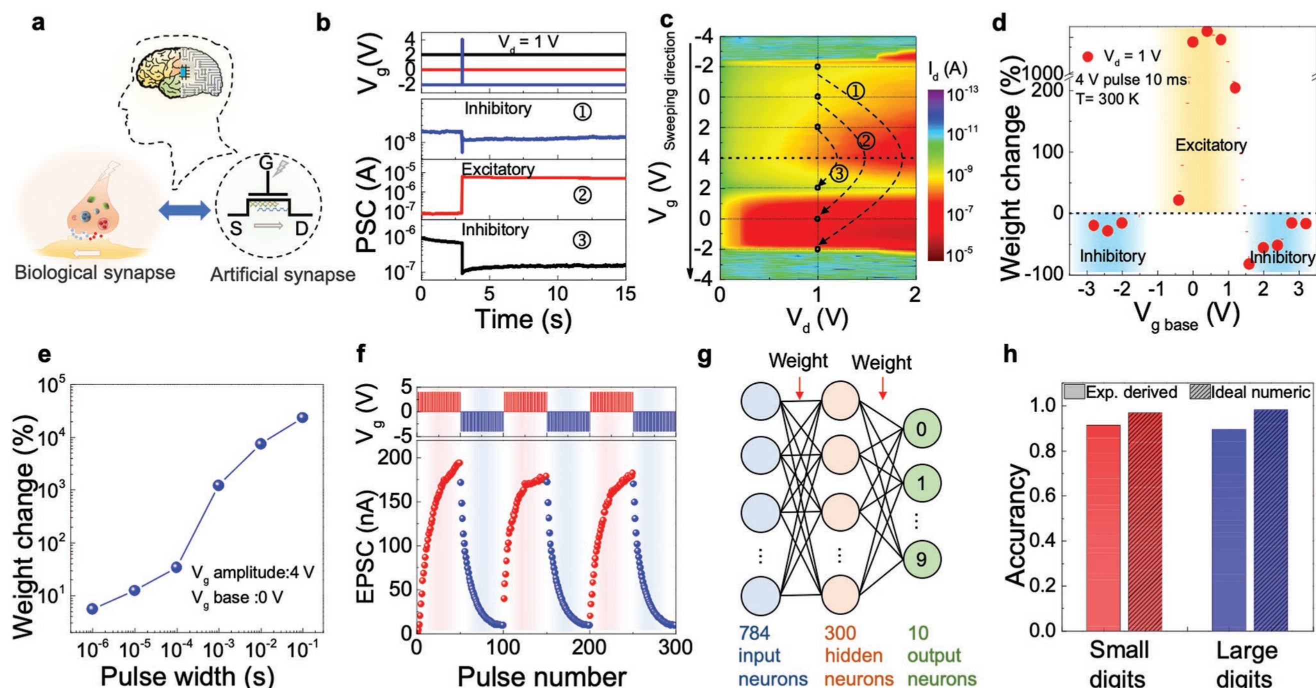

Figure 4. Artificial electric trilingual synapse based on BP/ReS_2 heterostructure. a) Schematic of a biological synapse and artificial synapse. b) PSC in response to a 4 V input pulse (10 ms) at the input terminal for three different V_{g_base} conditions of –2, 0, and 2 V. c) The measurement direction dependence of the drain current at different V_g and V_d. Three different V_g conditions show the variation tendency, corresponding to the points 1–3 in panel (b). d) Synaptic weight changes in response to a 4 V input pulse (10 ms) at different V_{g_base} conditions for V_d = 1 V at 300 K. e) Synaptic weight changes in response to a 4 V input pulse at different pulse width conditions for V_d = 1 V and V_{g_base} = 0 V at 300 K. f) Long-term potentiation and depression of the synaptic heterostructures using 50 potentiations (4 V, 100 µs) and depressions (–4 V, 10 µs) presynaptic input with V_d = 0.5 V. g) Schematics of a three-layer (one hidden layer) neural network. h) The recognition accuracy for small and large handwritten digit image with experimental devices and ideal numeric.

using experimental results of long-term plasticity characteristics in Figure 4f are benchmarked with ideal floating-point numeric precision that represents the neuromorphic algorithm limit, as shown in Figure 4h. The recognition accuracies of the small and large digits can finally reach ≈91.3% and 89.5% after 40 epochs, lower than the ideal numeric accuracies of ≈96.7% and 98.1%. The accuracy differences between the experiment-derived and the ideal numeric comes from the nonlinear and asymmetrical conductance change in LTP and LTD processes, which can be further improved with an optimized charge trapping layer.

3. Conclusion

In conclusion, we systematically study the multifunctional van der Waals heterostructures based on BP and ReS_2. The ternary nonvolatile inverter has been demonstrated for low power electronics with much a smaller footprint than conventional technology. Furthermore, the tunable artificial electronic synapses were carried out with a record high synaptic weight change over 10^4%. The neural network simulation for handwritten digits recognition based on the heterostructure devices were successfully implemented with a recognition accuracy of around 90%. These findings show great promise of the 2D logic-in-memory devices for future high-performance low-power computing.

4. Experimental Section

Device Fabrication: A P++-doped silicon wafer was selected as the substrate. The HfO_2 of ≈25 nm was then deposited as the back gate oxide by the atomic layer deposition system (Beneq TFS 200) at 250 °C. The flakes of BP and ReS_2 were obtained by mechanical exfoliation and aligned carefully by the dry transfer method. The contact electrodes were obtained using standard EBL and metal deposition techniques. Finally, additional atmospheric exposure oxidized the BP interface to form 4 nm thick PO_x. After that, the samples were always kept in the glove box where the oxygen and water contents were always kept below 0.1 ppm.

TEM Images: A cross-sectional specimen of the device was prepared by using a lift-out process in a dual-beam FEI Helios NanoLab G3 focus ion beam system. A Cr layer of about 15 nm was first deposited onto the samples' surface to increase the electrical conductivity. The TEM images of the sample were then obtained using Talos F200S high-resolution TEM.

Electrical Characterizations: Electrical measurements were carried out using Agilent B1500A semiconductor parameter analyzer. The pulse voltage was generated by the semiconductor pulse generator unit module. During all of the characterization, the device was placed inside a Lakeshore cryogenic probe station in the vacuum (<2 × 10^{-4} mbar). Liquid helium was used for cryogenic measurements.

Neural Network Simulations: The simulation of arrays devices for digital recognition by the ANN was performed in CrossSim platform,[45] which provided a clear python application programming interface. For the large digits dataset, the size of the network was 748 × 300 × 10, 60 000 samples for training the neural network and 10 000 samples for testing the accuracy. For the small digits dataset, the size of the network is 64 × 30 × 10, 3823 samples for training the neural network and 1797 samples for testing the accuracy.

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Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

2D devices, artificial neural networks, multilingual synapses, nonvolatile ternary logic, van der Waals heterostructures

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