Scaling of InGaAs MOSFETs into deep-submicron regime (invited)

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We have demonstrated high-performance deep-submicron inversion-mode InGaAs MOSFETs with gate lengths down to 150 nm with record G_m exceeding 1.1 mS/μm. Oxide thickness scaling is performed to improve the on-state/off-state performance and G_m is further improved to 1.3 mS/μm. HBr pre-cleaning, retro-grade structure and halo-implantation processes are first time introduced into III-V MOSFETs to steadily improve high-*k*/InGaAs interface quality and on-state/off-state performance of the devices. We have also demonstrated the first well-behaved inversion-mode InGaAs FinFET with ALD Al_2O_3 as gate dielectric using novel damage-free etching techniques. Detailed analysis of SS, DIBL and V_T roll-off are carried out on FinFETs with L_{ch} down to 100 nm and W_{Fin} down to 40 nm. The short-channel effect (SCE) of planar InGaAs MOSFETs is greatly improved by the 3D structure design. The result confirms that the newly developed dry/wet etching process produces damage-free InGaAs sidewalls and the high-k/3D InGaAs interface is comparable to the 2D case. Finally, ultra-shallow doping for V_T adjustment in deep submicron InGaAs MOSFETs using sulfur monolayers is demonstrated. This brings new potential solution to ultra-shallow junction formation for the further scaling of III-V MOSFETs.

I. Introduction

In the quest for perfect dielectrics for III-V semiconductors, significant progress has been made recently on inversion-type enhancement-mode InGaAs NMOSFETs, operating under the same mechanism as Si MOSFETs, using high-k gate dielectrics. The promising dielectric options include ALD Al_2O, HfO_2, HfAlO, ZrO_2 and in-situ MBE $Ga_2O_3(Gd_2O_3)$. Most recently, record-high inversion current above 1 A/mm has been achieved for long-channel Al_2O_3/InGaAs MOSFETs. In order to further verify the potential of scaling of the InGaAs MOSFETs towards the deep-submicron regime, we have made the surface channel inversion-type InGaAs MOSFETs with gate lengths down to 150 nm using electron beam lithography (EBL), and performed various techniques including oxide thickness scaling, channel engineering, novel surface treatment and 3-dimensional InGaAs FinFET with Fin width down to 40nm. These devices are compared in terms of the on-state performance and off-state performance. The results show that these InGaAs surface channel MOSFETs have great potential for next generation high performance applications.

II. Oxide Thickness Scaling of InGaAs MOSFETs

Fig.1 illustrates the cross section of an ALD $Al_2O_3/In_{0.75}Ga_{0.25}As$ MOSFET. A 500 nm p-type 4×10^{17} /cm^3 buffer layer, a 300 nm p-type 1×10^{17} /cm^3 $In_{0.53}Ga_{0.47}As$ layer, and a 12 nm strained p-type 1×10^{17} /cm^3 $In_{0.75}Ga_{0.25}As$ channel were sequentially grown by molecular beam epitaxy on a 2-inch p^+-InP wafer. Fig. 2 shows the process flow for the Inversion-type Enhancement-mode InGaAs MOSFET. After surface cleaning and ammonia passivation, the wafers were transferred via room ambient to an ASM F-120 ALD reactor. A 10 nm thick Al_2O_3 encapsulation layer was deposited at a substrate temperature of 300°C. All patterns were defined by a Vistec VB-6 UHR EBL system. The source and drain regions of the MOSFETs were formed by selective implantation of 1×10^{14} cm^{-2} at 20 keV Si and annealed at 600°C - 700°C for 10 s in N_2 for activation. Relatively low implantation energy was chosen here to avoid the penetration of implanted Si ions through the 280 nm thick electron beam resist used to protect the channel regions.

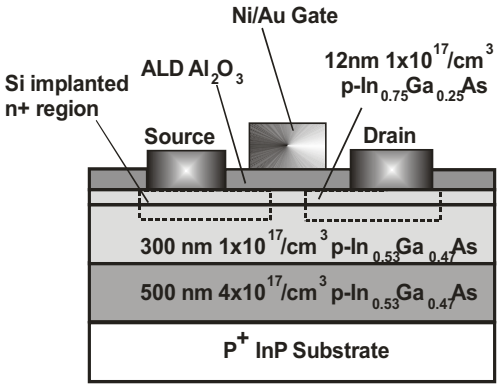

Fig. 1 Cross-section schematic view of InGaAs MOSFET.

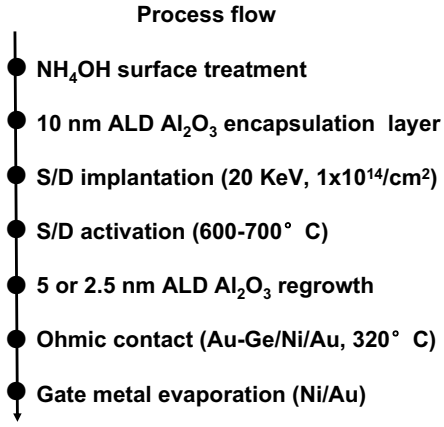

Fig. 2 Process flow of the Inversion-type Enhancement-mode InGaAs MOSFET.

After treated with $(NH_4)_2S$ solution for 10 minutes, another 5 nm Al_2O_3 or 2.5 nm Al_2O_3 was also grown by ALD after stripping away the encapsulation oxide layer. The ohmic source and drain contacts were made by electron-beam evaporation of AuGe/Ni/Au and annealing at 320°C for 30 s in N_2. The gate electrode was made by electron-beam evaporation of Ni/Au. The fabricated MOSFETs have nominal gate lengths L_g of 100, 110, 120, 130, 140, 150, 160, 170, 180 and 200 nm defined by the source-drain implant separation. The device process is not self-aligned.

The oxide thickness scaling has been introduced to explore the potential for the complete scaling. Reduction of Al_2O_3 down to 2.5 nm (EOT≈1nm) can improve the electrostatic control of the channel significantly, and can increase the electric field to the semiconductor surface at similar voltage supply. A typical 160 nm-gate-length inversion-mode $In_{0.7}Ga_{0.3}As$ NMOSFET with 5 nm Al_2O_3 as gate dielectric shows a I_{dss} of 840 μA/μm and peak G_m of 650 μS/μm at maximum supply voltage of V_{DD}=1.6 V. The contact resistance R_C of 350 Ω·μm is measured by TLM. After subtracting the contact resistance, the resulting intrinsic G_m is as high as 840 μS/μm. A similarly finished 160 nm-gate-length inversion-mode $In_{0.7}Ga_{0.3}As$ NMOSFET with 2.5 nm Al_2O_3 as gate dielectric shows I_{dss} of 810 μA/μm and peak G_m of 1100 μS/μm at maximum supply voltage of V_{DD}=1.6 V. After subtracting the contact resistance, the resulting intrinsic G_m is as high as 1790 μS/μm. The V_T shifts positively almost 0.5V as can be seen in the later part of this paper.

Fig. 3 compare I_{dss} and G_m of 2.5 nm and 5 nm Al_2O_3 devices without HBr treatment at V_{DD}=1.6V. Record high extrinsic transconductance G_m of 1.3 mS/μm is reached at L_{ch}=150 nm. Both the I_{dss} and G_m of the 2.5nm devices are significantly improved over the 5nm devices. Especially for the transconductance, the improvement is more than 50% for long channel devices and more than 80% for the shorter channel devices (channel lengths less than 170 nm). This shows the great potential InGaAs MOSFETs have in terms of the gate stack scaling.

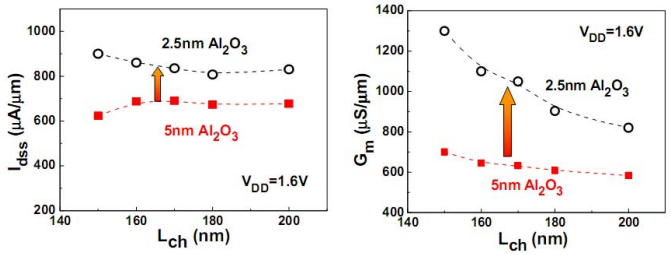

Fig. 3 Comparison of I_{dss} and G_m vs L_{ch} for devices with 2.5nm and 5nm thick gate dielecrics w/o HBr pretreatment and at V_{ds}=1.6V

Improved off-state characteristics are summarized in Fig. 4. S.S. improves through the better gate control by reducing the effect from the interface trap capacitance. Both the SS and DIBL show great potential to be further improved to be comparable with Silicon with better gate control. This comparison shows the potential of both on-state and off-state performance of the deep-submicron InGaAs MOSFETs for logic applications. The availability of even higher dielectric constant material, i.e., ALD $LaLuO_3$ (k=24-26), provides a pathway to further scale down the InGaAs MOSFETs.

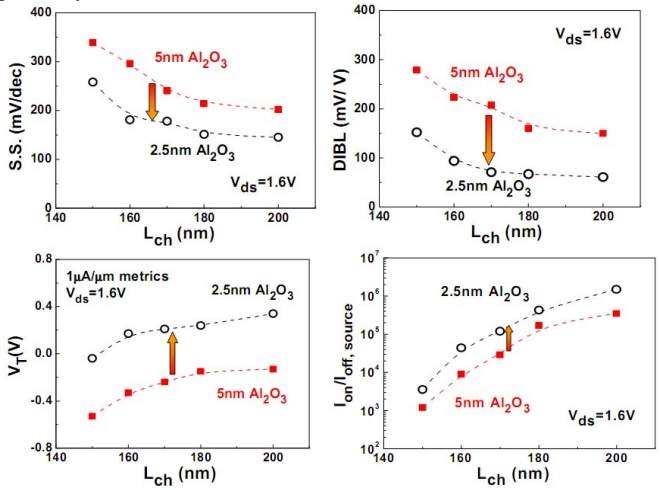

Fig. 4 Comparison of SS, DIBL, V_T and I_{on}/I_{off} vs. L_{ch} for the devices with 2.5nm and 5nm Al_2O_3.

III. Novel HBr Surface Pretreatment for InGaAs MOSFETs

The interface quality between the gate oxide and III-V

channel material is commonly regarded as one of the major challenges for high performance III-V MOSFETs. Although the ALD process has a self cleaning mechanism and can effectively reduce the interface trap density, it is one of the major causes for degrading transistor performance due to the contribution of C_{it}. To further improve the interface quality between ALD oxide and InGaAs channel, novel HBr / $(NH_4)_2S$ has been proposed in order to get better on-state performance as well as off-state performance.

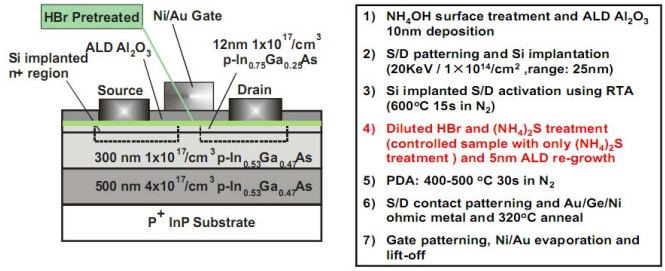

Fig. 5 Cross section schematic view and process flow of the HBr treated InGaAs MOSFET

Fig. 5 show the schematic cross section of HBr treated MOSFETs. ALD Al_2O_3 as gate dielectric was grown directly on MBE InGaAs surface. A 500 nm p-doped 4×10^{17} cm^{-3} buffer layer, a 300 nm p-doped 1×10^{17} cm^{-3} $In_{0.53}Ga_{0.47}As$ and a 12 nm 1×10^{17} cm^{-3} $In_{0.7}Ga_{0.3}As$ channel layer were sequentially grown by MBE on a 2-inch InP p+ substrate for all samples except for the retro-grade sample. The process flow is shown in Fig. 14. After surface degreasing and ammonia-based native oxide etching, the wafers were transferred via room ambient to an ASM F-120 ALD reactor. A 10 nm thick Al_2O_3 layer was deposited at a substrate temperature of 300 °C as an encapsulation layer after NH_4OH treatment. Source and drain regions were selectively implanted with a Si dose of 1×10^{14} cm^{-2} at 20 keV through the 10 nm thick Al_2O_3 layer. The implantation condition was chosen carefully to achieve the desired junction depth and S/D doping concentration. Implantation activation was achieved by rapid thermal anneal (RTA) at 600 °C for 15 s in a N_2 ambient. After removing the 10nm oxide in BOE, HBr / $(NH_4)_2S$ combination was used as the novel pretreatment and followed by another 5nm Al_2O_3 growth by ALD. HBr treated InGaAs surface is hydrophilic and is believed to be helpful to passivate InGaAs surface from surface recombination velocity measurements [16]. And it is expected to improve interface properties and the output performance. After 400-500 °C PDA process, the source and drain ohmic contacts were made by an electron beam evaporation of a combination of AuGe/Ni/Au and a lift-off process, followed by a RTA process at 320 °C for 30 s also in a N_2 ambient. The PDA temperature cannot exceed 500°C, as the remaining Sulfur atoms on the interface will be activated and serve as an n-type doping at temperatures above 600°C. The gate electrode was defined by electron beam evaporation of Ni/Au and a lift-off process.

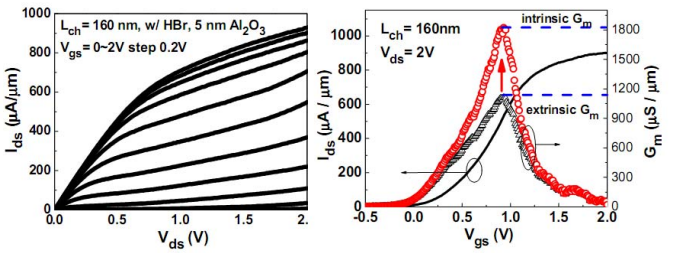

Fig. 6 output and transfer characteristic of an HBr treated 160 nm InGaAs MOSFET with 5nm Al_2O_3.

A well-behaved I-V characteristic of a 160 nm-gate-length inversion-mode $In_{0.7}Ga_{0.3}As$ NMOSFET with 5 nm Al_2O_3 as gate dielectric is demonstrated in Fig. 6 with I_{dss} of 925 μA/μm and peak G_m of 1.1 mS/μm at maximum supply voltage of V_{DD}=2.0V. The contact resistance R_C of 350 Ω·μm is measured by TLM. After subtracting the contact resistance, the resulting intrinsic G_m is as high as 1.8 mS/μm.

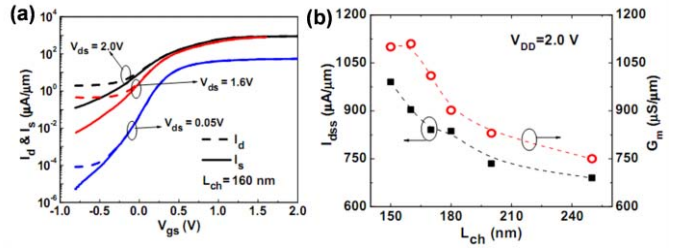

Fig. 7 (a) I_d and I_s at three V_{ds} of the same $In_{0.7}Ga_{0.3}As$ MOSFET with L_{ch}=160nm. (b) scaling characteristics of maximum drain current and peak transconductance vs L_{ch}

Fig. 7(a) shows I_d and I_s at V_{ds}=2.0V, 1.6V and 0.05V, respectively. It is clear that I_{sub} (the reverse-biased pn-junction leakage current) determines the leakage floor and I_d at $V_{gs} < 0$ as discussed before caused by the implantation and activation steps. The off-state is thus affected adversely by this parasitic effect. There is no Fermi-level pinning at $V_{gs} < 0$ since the gate still controls the channel well as shown in Is with 7-8 orders of magnitude change with the gate bias. The analysis on I_s reflects more accurately the intrinsic properties of devices by avoiding the substrate leakage. The major contribution of the difference of drain and source current comes from the non-optimized S/D junctions, which can be improved by the refined implant condition and following thermal activation. Fig. 7(b) summarizes the increase of I_{dss} and G_m, the on-state performance, versus the channel length L_{ch} from 250 nm to 150 nm. The maximum drain current changes from 700 μA/μm to 1 mA/μm and peak transconductance changes from 750 μS/μm to more than 1 mS/μm as the gate length scales. It shows pretty good trend of increasing output performance while scaling the channel length, which is promising for further scaling into the nanometer regime.

IV. Channel Engineering for InGaAs MOSFETs

Channel engineering–retro-grade structure and halo-implantation–has been studied to further improve off-state performance. The underlying heavily doped InGaAs layer beneath the channel of the retro-grade structure would

improve the S/D punch-through. The halo-implantation was performed by implanting Zn with ±30 degree angles to the normal.

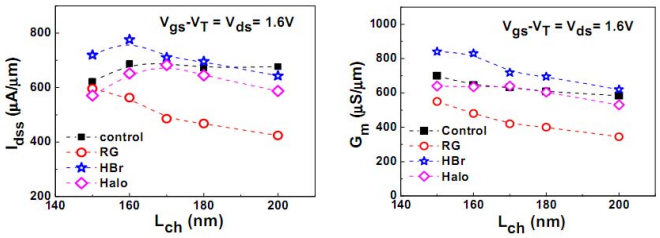

Fig. 8 Comparison of I_{dss}, G_m vs L_{ch} for 4 different types of channel engineering.

Fig. 8 summarize I_{dss} and G_m of 4 different types of devices with 5 nm Al_2O_3 at all L_{ch} measured. Uniform channel as shown in Fig. 1 without HBr pretreatment is used as a control sample. HBr treated sample (without channel engineering) has the best on-performance among the four and is attributed to the improved interface. Both retro-grade sample and halo-implanted sample are degraded on-current and peak G_m, which are expected from inducing scattering and reducing channel mobility. This is a trade-off for the improved off-state performance such as S.S. and DIBL as demonstrated in Fig. 9.

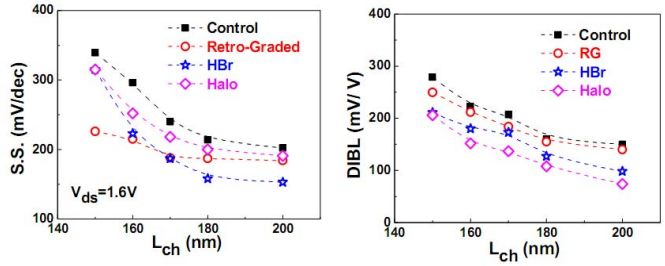

Fig. 9 Comparison of SS, DIBL vs L_{ch} for 4 different types of channel engineering

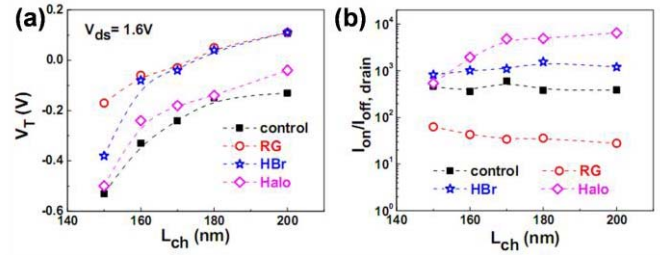

Fig. 10 Comparison of (a) V_T and (b) I_{on}/I_{off} obatained from 4 different channel engineering.

Fig. 10(a) shows V_T vs L_{ch} using I_{ds}=1μA/μm metrics at V_{ds}=1.6V. The typical roll-off of V_T at shorter gate lengths is also observed here. All treated samples have better V_T roll-off than control sample. Fig. 10(b) summarizes I_{on}/I_{off} vs L_{ch} of 4 different types of devices from I_d. I_{on}/I_{off} is chosen as I_{on} (V_{ds}=1.6V, V_{gs}=2/3V_{ds}+V_T)/I_{off} (V_{ds}=1.6V, V_{gs}=-1/3V_{ds}+V_T), where V_T is determined by 1μA/μm metric. The similar definition is also used for Is. Junction leakage is the dominant factor currently for I_d at V_{gs}<0 or I_{off}. For retro-grade sample, I_{sub} or I_{off} is higher due to heavily p-doped 2×10^{18}/cm^3 layer in source/drain. This junction leakage mainly comes from the non-optimized S/D junctions after implantation and activation which can be greatly improved by better control of the process. If eliminating the junction leakage or I_{on}/I_{off} taken from I_s, I_{on}/I_{off} is improved to 104-106 at 150-200 nm gate lengths. Without considering the contribution from short-channel effect, with the lowest S.S. of 126 mV/dec. For HBr treated samples at V_{ds}=0.05V, the upper limit for interface trap density D_{it} is $2.8\text{x}10^{12}$/cm^2-eV. The short-channel effect will significantly degrade SS when the gate lengths get shorter. The first pitfall introduced in calculating D_{it} directly from SS comes from SCE, especially in the deep submicron region. The deteriorating of SS for short devices could be attributed to the enhanced SCE by adding a term of CGD, which is a function of drain induced barrier lowering. With DIBL of less than 100 mV/V, it is reasonable to assume the SCE is minimized for 250 nm long device. More detailed interface characterizations by CV and GV methods are on-going to more accurately to determine the interface properties of the deeply scaled InGaAs MOSFETs.

V. 3D structure: InGaAs FinFET

With the continuous request of carrier transport boosting in CMOS devices, very recently, much progress has been made on achieving on-state performance of inversion-mode In–rich InGaAs MOSFETs using high-k gate dielectrics. However, the off-state performance of InGaAs MOSFETs is far from satisfactory according to ITRS requirement. The short-channel effect (SCE) of InGaAs MOSFETs deteriorates more quickly than Si MOSFETs due to its nature of narrower bandgap and higher semiconductor dielectric constant. In order to achieve better gate control capability, new structure design like FinFET demonstrated successfully in Si devices, is strongly needed for short-channel III-V MOSFETs. However, unlike Si, the dry etching of III-V semiconductor surface has been believed to be difficult and uncontrollable, especially related with surface damage and integration with high-k dielectrics. In this paper, we report for the first experimental demonstration of inversion-mode $In_{0.53}Ga_{0.37}As$ tri-gate FinFET using damage-free etching and ALD Al_2O_3 as gate dielectric. The SCE is greatly suppressed in terms of SS, DIBL and V_T roll-off. Detailed analysis and comparison are performed on the FinFETs with channel length (L_{ch}) from 200 nm to 100 nm, fin width (W_{Fin}) from 100 nm to 40 nm, and fixed fin height (H_{Fin}) of 40 nm. The reduction in the SCE shows the great promise for InGaAs transistors to continue scale into the sub-100nm regime. Fig. 11 shows the schematic cross section of the uniform device structure and the device fabrication flow. A 500 nm p-doped 2×10^{18} cm^{-3} InP layer, a 300 nm p-doped 2×10^{16} cm^{-3} and a 40 nm 2×10^{16} cm^{-3} $In_{0.53}Ga_{0.47}As$ channel layer were sequentially grown by MBE on a 2-inch InP p+ substrate. The heavily doped InP layer beneath the channel was chosen to prevent punch through and reduce substrate leakage because of its higher bandgap.

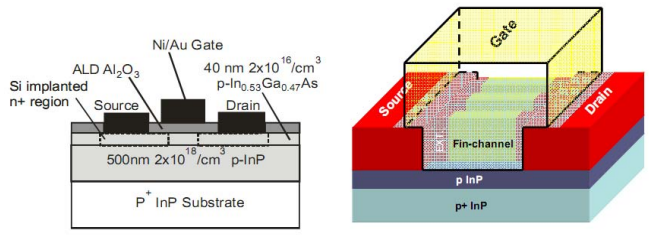

Fig. 11 Cross section schematic view and 3-dimensional schematic view of the InGaAs FinFET

Due to the non-optimized source/drain junctions, the heavily doped InP layer resulted in worsen junction leakage. After surface degreasing and ammonia-based native oxide etching, the wafers were transferred via room ambient to an ASM F-120 ALD reactor.. A 10 nm thick Al_2O_3 layer was deposited at a substrate temperature of 300°C as an encapsulation layer. Source and drain regions were selectively implanted with a Si dose of 1×10^{14} cm^{-2} at 20 keV through the 10 nm thick Al_2O_3 layer. The implantation condition was chosen carefully to achieve the desired junction depth and S/D doping concentration. Implantation activation was achieved by RTA at 600 °C for 15 s in a nitrogen ambient. The reduction of activation temperature from 750 °C to 600 °C resulted in much improved S/D junction leakage while achieving similar activation efficiency.

A combined dry and wet etching was used to pattern the fin structures. High-density plasma etcher (HDPE) BCl_3/Ar was used for dry etching at the chamber pressure of 2 mTorr. The gas flow of BCl_3/Ar is 15 sccm/ 60 sccm and the RF source power and bias power is 100 w and 50 w, respectively. The achieved etching rate for InGaAs under this condition is estimated to be 20nm / min. The positive E-beam resist ZEP-520A was used as an etching mask in this case. To achieve the desired small feature of 40nm, the original ZEP 520A resist was diluted with A-thinner (anisole) at the ratio of 1:0.7. The resist thickness of the diluted ZEP 520A is around 200nm at a spinning speed of 2000 rpm. A short dip of 3 seconds in diluted H_2SO_4:H_2O_2:H_2O (1:8:400) solution was carried out immediately after the dry etching to remove the damaged surface layer. The resulted fin channels have a depth of 40 nm which can be seen from the last SEM image in Fig. 12.

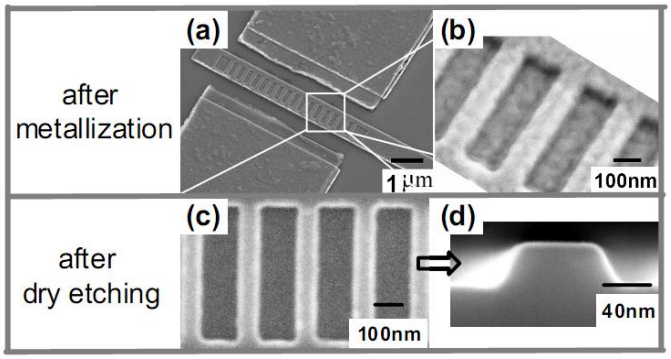

Fig. 12 (1) Tiled SEM of a finished FinFET device (b) Zoomed in image of the channel region with gate dielectric and gate metal (c) SEM image of the Fin structure after dry etching (d) Cross section SEM image of a Fin after dry etching

More sophisticated process is needed to make the fin side-walls perfectly vertical. A 5 nm Al_2O_3 film was regrown by ALD after removing the encapsulation layer by BOE solution and $(NH_4)_2S$ surface preparation. After 400-500 °C PDA process, the source and drain ohmic contacts were made by an electron-beam evaporation of a combination of AuGe/Ni/Au and a lift-off process, followed by a RTA process at 320 °C for 30 s also in a N_2 ambient. The gate electrode was deposited by electron- beam evaporation of Ni/Au and a lift-off process. The fabricated MOSFETs have a nominal gate length varying from 100 nm to 150 nm and fin widths from 40 nm to 100 nm. From the SEM images of Fig. 12 (a) and (b), the gate metal covers uniformly on the parallel multi-fin channels. All patterns were defined by a Vistec VB-6 UHR electron-beam lithography (EBL) system. A Keithley 4200 was used for MOSFET output characteristics. The combined dry and wet etching for the formation of fin channels results in damage-free sidewalls. It is verified by the carrier transport through the fin channels without any significant degradation, compared to the planar devices. Fig. 13 depict the well-behaved output characteristic of a FinFET with 40 nm and 100nm W_{Fin} at same channel length of 100nm. There is no significant reduction of drain current even when the fin width is reduced down to 40 nm dimension. Note the current density is scaled by the fin width plus 2 x fin heights. Fig. 14(a) shows the typical output characteristics of a planar 100 nm-long MOSFET. It cannot be turned off at zero gate bias due to the SCE. Fig. 14(b) depicts the well-behaved output characteristic of a FinFET with 40 nm W_{Fin} at same channel length. From the comparison, it clearly shows the FinFET has much better behaved output characteristics in terms of off-state while maintaining the on-state performance compared to the planar device.

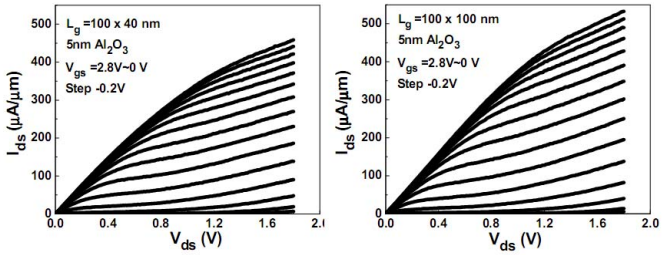

Fig. 13 I_{ds} vs V_{ds} of a FinFET with L_{ch}=100nm and W_{fin} = 40nm or 100nm.

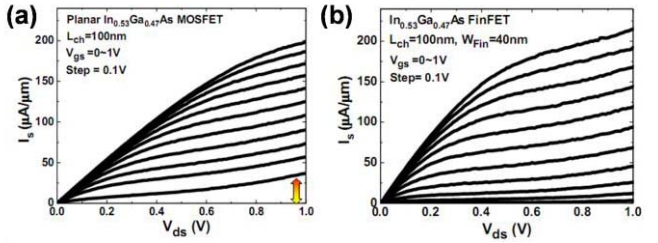

Fig. 14 I_s vs V_{ds} of a (a) Planar MOSFET with L_{ch}=100nm and (b) FinFET device with L_{ch} =100nm and W_{Fin}=40nm.

SS from the saturation region as well as DIBL are compared among FinFETs with 4 different WFin from 40 nm to 100 nm and the planar FET in Fig. 15. The trend shows the

device with narrower WFin has better SS and DIBL as expected. The SS of FinFET with 100 nm channel length improves more than 34% percent and degrades much slower when channel length gets shorter. The DIBL is greatly reduced from 440 mV/V for the planar device to 180 mV/V for the FinFET at 100 nm gate length.

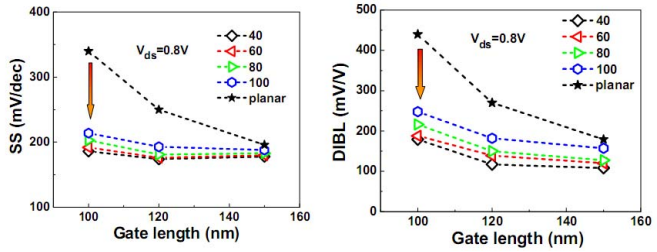

Fig. 15 Comparison of SS and DIBL of FinFETs and Planar FETs.

In order to evaluate the sidewall quality after the dry/wet etching, it is common to estimate the interface trap density (D_{it}) from SS. The channel surfaces of FinFET should be not better than the planar devices, if not worse after going through all the patterning and etching processes. From Fig. 36, it is clear that the SS is not only affected by interface trap density, but also by SCE. Simple estimation of D_{it} from SS would result in gross overestimation. The results show the linear region, similarly as in saturation region, SS of FinFETs are lower than those from the planar FET even in the 150 nm channel device which has small SCE. This indicates that the interface properties of Al_2O_3/InGaAs on the etched sidewalls are not degraded much by the Fin etching process, or D_{it} on the sidewalls is not much larger than that on the planar structures. It verifies that the newly developed dry/wet etching process is *damage-free* and suitable for 3D III-V device fabrication. The upper limit of average D_{it} on the top and sidewall surfaces in $In_{0.53}Ga_{0.47}As$ FinFET is $1.7x10^{12}/cm^2$-eV. The similar trend is also observed from the simple calculation of SS vs. W_{Fin}/L_{ch} as a function of D_{it}. The result confirms that the newly developed dry/wet etching process produces damage-free InGaAs sidewalls and the high-k/3D InGaAs interface is comparable to the 2D case.

VI. Sulfur doping effect for V_T adjustment

We study the thermal stability of the $(NH_4)_2S$ treatment by adding two different S activation annealing step in our gate-last $In_{0.75}Ga_{0.25}As$ devices. After S/D activation at 600°C and removing the encapsulation Al_2O_3 layer, $(NH_4)_2S$ solution is used to passivate the surface. The samples were transferred to an ALD chamber immediately for 5nm ALD regrowth. Previous XPS studies show that after ALD growth, part of sulfur still exists at high-*k*/III-V interface. Two different S activation anneal were carried out at 400°C or 600°C after gate oxide deposition. Fig. 16 (a) shows the linear regime threshold voltage extracted for these gate-last devices. Devices annealed at 600°C with variable gate lengths exhibits a ~-0.35V V_T shift compared to the ones annealed at 400°C. This is consistent with the split CV measurement results shown in Fig. 16 (b), showing a similar negative V_T shift on the C_{gs}-V_g curve. This indicates that the PDA process at 600°C partially activated the S layer at the interface, introducing extra negative charge that promotes inversion.

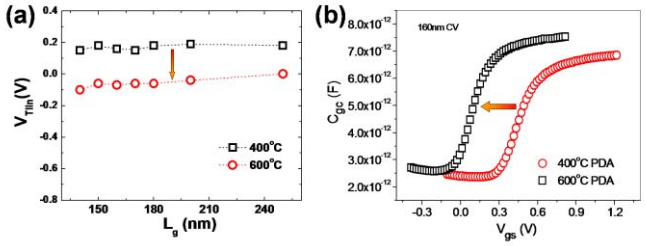

Fig. 16 (a) linear extrapolated V_T and (b) Split CV measurement of gate-last InGaAs devices with 400°C or 600°C PDA after gate oxide deposition.

In conclusion, threshold voltage adjustment has been realized by activating the sulfur surface layer. The same technique can be used to form ultra-shallow junctions of S/D, providing a solution for the further scaling of III-V MOSFETs.

VII. Conclusion

In summary, we have demonstrated high-performance deep-submicron inversion-mode InGaAs MOSFETs with record G_m exceeding 1.1 mS/μm. HBr pre-cleaning, retro-grade structure and halo-implantation processes are first time introduced into III-V MOSFETs to steadily improve high-k/InGaAs interface quality and on-state/off-state performance of the devices. We have also demonstrated the first well-behaved inversion-mode InGaAs FinFET with ALD Al_2O_3 as gate dielectric. Detailed analysis of SS, DIBL and V_T roll-off are carried out on FinFETs with L_{ch} down to 100 nm and W_{Fin} down to 40 nm. The SCE of planar InGaAs MOSFETs is greatly improved by the 3D structure design. Much more work on high-k/InGaAs interface and InGaAs ultra-shallow junction are needed to make III-V an alternative technology at CMOS 15 nm technology node.

Acknowledgment

The work is supported by National Science Foundation and SRC FCRP MSD Center. The authors thank D.A. Antoniadis for the valuable discussions.

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