BEOL Compatible 15-nm Channel Length Ultrathin Indium-Tin-Oxide Transistors with I_{on} = 970 μA/μm and On/off Ratio Near 10^{11} at V_{ds} = 0.5 V

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***Abstract*—**In this paper, we report high-speed ultrathin-body (3.5 nm) indium-tin-oxide (ITO) transistors using high-k HfLaO dielectrics with a thickness of 5 nm. Because of its low dielectric constant and large bandgap, ITO is a promising channel material for scaling below the 5 nm regime for advanced low-power electronics with excellent short-channel-immunity. Here, we fabricate sub-100-nm channel length ITO transistors with ultrahigh on/off ratio near 10^{11} and ultralow off-state current below 10 fA/μm. The 15-nm-long ITO transistor exhibits high performance with the maximum on-state current of 970 μA/μm and peak g_m of 400 μS/μm at V_{ds} = 0.5 V. NAND, NOR, and SRAM based on enhancement/depletion mode (E/D) inverters have achieved full rail-to-rail output characteristics and stable memory function. Finally, We demonstrated a stage delay of 0.49 ns/stage for a 5-stage ring oscillator based on bootstrapped mode (BST) inverter, which is the best among all results based on metal-oxides transistors.

I. Introduction

Thin-film transistor is the cornerstone of low-power electronics with application from large-scale display to flexible portable devices [1]. Indium-tin-oxide (ITO), is well-known as a transparent conductive material and widely used in display application for transparent electrodes. A few reports have shown that the carrier density of ITO can be decreased by adjusting the oxygen vacancy which will transfer the degenerate semiconductor to non-degenerate semiconductor with efficient gate electro-static control [2]. However, none of these transistors can achieve a high on current while maintaining a high on-off ratio, especially at relative small V_{ds}, including the recent emerging two dimensional materials. In this work, we fabricated the ITO transistors with a staggered bottom gate device structure as shown in Fig. 1. Besides, we adopted 3.5-nm-thick channel and 5-nm-thick dielectric to ensure the short enough natural length ($\boldsymbol{\lambda = \sqrt{\frac{\varepsilon_s}{\varepsilon_i} t_s t_i}}$) for short-channel-immunity. The sub-100-nm ITO transistors all exhibit near 10^{11} on/off ratio with off-state current lower than 10 fA/μm which is beyond the measurement limit owing to the low dielectric constant and ultrathin body with large bandgap. The field-effect mobility of 54 cm^2/Vs further demonstrates the good material properties of 3.5-nm ITO, which is among the highest for such a thin amorphous film. Record high peak transconductance g_m of 400 μS/μm and I_{on} of 970 μA/μm at V_{ds} = 0.5 V can be achieved for a 15-nm-long ITO transistor, indicating its advantages in low-power application with high performance. Moreover, we fabricated NAND, NOR logic gates and SRAM based on E/D inverters. The NAND and NOR logic gates both show full rail-to-rail output characteristics, and SRAM operates with a stable memory function due to the good noise margin of ITO-based E/D inverter. To obtain an ultrafast stage delay, we used BST inverters to construct 5-stage ring oscillator with the record low stage delay of 0.49 ns/stage among the metal-oxides technology.

II. Device Structure and Fabrication

Fabrication process flow of ITO transistors is illustrated in Fig. 2. A high resistance (>10000 Ω·cm) silicon coupled with 90-nm silicon oxide (SiO_2) was used as the substrate. Then local inverted gates were patterned on the substrate using electron beam lithography (EBL), followed by a metallization process of 5/25 nm Ni/Au. La-doped Hafnium-oxide (HfLaO) was deposited by atomic layer deposition (ALD) as the gate oxide with alternating $Hf[N(CH_3)(C_2H_5)]_4$, $La((^iPr_2N)_2CH)_3$ and O_3 precursor pulses at 300 °C. The cycle ratio for HfO_2 and La_2O_3 was 8:1 with a total thickness of 5 nm HfLaO. Inductively coupled plasma (ICP) was employed to etch the oxide for gate pad opening. The etching gases were 25 sccm BCl_3 and 10 sccm Cl_2. The ICP power was 500 W and RF power was 75 W, with a chamber pressure of 10 mTorr. Next, channel regions were patterned by EBL, followed by ITO films deposition by magnetron assisted sputtering at 200 °C. The relative oxygen flow ratio ($[O_2]/[Ar+O_2]$) was 0.1. We fixed sputtering pressure at 0.15 Pa and radio-frequency forward power/reflection power of the ITO target (90wt.% In, 10wt.%Sn) at 60 W/ 1 W to control the deposition rate at 0.7 nm/min. After the ITO deposition, the substrate was immersed into PG remover to lift-off the ITO films outside the channel region. Finally, a stack of 5/30 nm Ni/Au for source and drain contacts were deposited.

III. Results and Discussion

The thickness of ITO film is around 3.5 nm measured by atomic force microscope (AFM) as shown in Fig. 3. Selected area electron diffraction (SAED) diffraction pattern of Fig. 4 and high-magnification transmission electron microscope

(TEM) image of Fig. 5 confirm the amorphous state of 3.5-nm ITO, which is suitable for uniformity requirement for large-scale fabrication. We extracted bandgap of 3.69 eV for 3.5-nm-ITO in Fig. 6, which is beneficial for minimizing the channel leakage current with a large potential barrier. The mobility as a function of carrier density is shown in Fig. 7. A peak field-effect mobility of 54 cm^2/Vs is obtained from 3.5-nm-ITO, which is much higher than the typical value of 10 cm^2/Vs for commercial IGZO and 1 cm^2/Vs for amorphous-Si, indicating excellent application potential of ITO transistors.

The scanning electron microscope (SEM) of 15-nm channel-length device is shown in Fig. 8. Output characteristics of the 15-nm-long ITO transistor are shown in Fig. 9. The on-state current can reach 970 μA/μm at V_{ds} = 0.5 V and V_{gs} = 2 V, exhibiting the good contact between ITO films and Ni electrodes and excellent transport property. Fig. 10 shows the transfer characteristics I_{ds}-V_{gs} of ITO transistors with channel-length varying from 15 nm to 90 nm at V_{ds} = 0.5 V. The ultralow off-state current below 10 fA/μm is beyond equipment measurement limit. The on/off ratio is near 10^{11} for all devices. Fig. 11 shows g_m versus V_{gs} at V_{ds} = 0.5 V for the same devices discussed in Fig 10. The highest g_m of 400 μS/μm is obtained for the 15-nm-long ITO transistor, which decreases as channel length increases. We compare the on current, on/off ratio, and g_m of ITO transistors with the best-reported metal-oxides-based and MoS_2-based (a representative 2D material) transistors with L_{ch} dependence, as shown in Fig. 12, Fig. 13 and Fig. 14, respectively [3-7]. The V_{ds} is 0.5 V for this work while it is 1 V~ 2 V for the references data. The I_{on} of the ITO transistors is much larger than all of the metal-oxides-based transistors, while it is 2 times larger than MoS_2-based transistors in the sub-20-nm region. With the scaling of the channel length, the I_{on} exhibits a monotonic increase, showing shows the channel length scaling benefit of the ITO transistors. The on/off ratio maintains near 11 decades for ITO transistors with channel length from 15 nm to 90 nm, much better than metal-oxides and MoS_2. The lower off-state current, the lower is the dissipation power at standby state, demonstrating the promising future for ITO transistors in the low-power application. As shown in Fig. 14, The transconductance of these ITO transistors decreases from 400 μS/μm to 240 μS/μm as the channel length increases, which is still much larger than the best of metal-oxides and MoS_2 at similar channel lengths.

Fig. 15 shows the equivalent circuit and optical micrograph of the E/D mode inverter. The channel length of load and drive transistor is 0.1 μm and 0.5 μm, respectively, while their channel width is both 10 μm. Fig. 16 shows the output characteristics of the E/D inverter. The red line shows when V_{in} = V_{out} meets the E/D inverter's output line at 1/2 V_{dd}, enabling a good noise margin. The transient characteristics and corresponding circuit structures of NAND, NOR are shown in Fig. 17, Fig. 18 respectively. The voltage level of logic 1 is 2 V, while it is 0 V for logic 0. For NAND logic gate, the output maintains logic 1 if one of the inputs is logic 0, which means at least one transistor is turned off. The output logic 0 state can only be obtained when both ITO transistors are turned on. As for NOR logic gate, logic 0 is obtained as long as once input logic is high, and logic 1 can only be obtained when both inputs are low. The logic gate NAND and NOR both achieve a decent rail-to-rail operation in this work. The SRAM transient characteristics and corresponding circuit structures are shown in Fig. 19. If we open the input switch after a period of input voltage 1, the output voltage can stay at 0 state. And it can remain the output 1 state after the input logic 0 has been opened, indicating a stable memory function for SRAM [8].

Other than E/D inverter, BST inverter has been demonstrated in Fig. 20. There is a pre-charge transistor in addition to the normal load and drive transistors, which helps to boost the output voltage with the ground input level. The channel lengths of 3 transistors are 0.4 μm, while the channel widths are 1 μm, 10 μm and 50 μm for the pre-charge transistor, load transistor, and drive transistor, respectively. We used such BST inverters to construct a 5-stage ring oscillator. There is a buffer stage at the end of the 5-stage ring oscillator to segregate the output and input signal as shown in Fig. 21. Fig. 22 and Fig. 23 show the output waveform of a 5-stage ring oscillator with BST inverter at V_{dd} = 4 V in the time domain and frequency domain, respectively. The output frequency is 176 MHz for 5-stage ring oscillator at V_{dd} = 4 V, while it is 206 MHz at V_{dd} = 4.5 V as shown in Fig. 24 and Fig. 25. We summarized stage delay as a function of V_{dd} in Fig. 26 in comparison with literature from 2007 to 2019 [9, 10]. We achieved the fastest stage delay of 0.49 ns/stage, which is over 2 times faster than the best result in previous works based on metal-oxides.

IV. CONCLUSIONS

High-speed 3.5-nm-ITO transistors using high-k HfLaO dielectrics with t_{oxide} 5 nm were fabricated in this work. The record-high on-state current of 970 μA/μm, transconductance of 400 μS/μm and on/off ratio near 10^{11} have been successfully demonstrated for 15-nm channel-length ITO transistor. Logic gates of NAND and NOR based on ITO transistors have achieved full rail-to-rail output characteristics. The SRAM has also operated with a stable memory function. The high-performance 5-stage ring oscillator with record-fast stage delay of 0.49 ns/stage is achieved. These figures of merit indicate the remarkable potential of the ITO-based transistors for future low-power, high-performance, and high-frequency applications.

ACKNOWLEDGMENT

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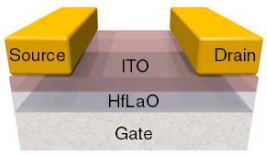

Fig. 1. Schematic of the 3.5-nm indium-tin-oxide inverted gate transistor. The gate dielectric is 5-nm HfLaO.

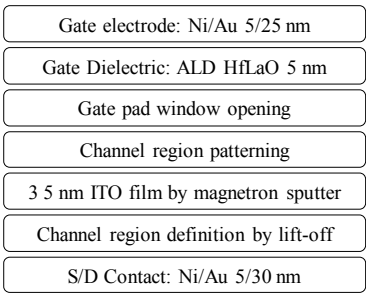

Fig. 2. Fabrication process flow of the ITO transistors.

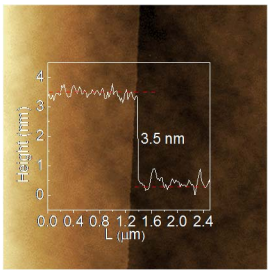

Fig. 3. AFM image of ITO films with a thickness of 3.5 nm.

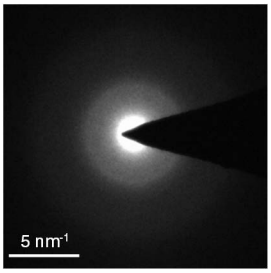

Fig. 4. SAED diffraction pattern of amorphous ITO films.

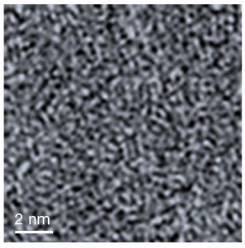

Fig. 5. High-magnification TEM image of amorphous ITO films.

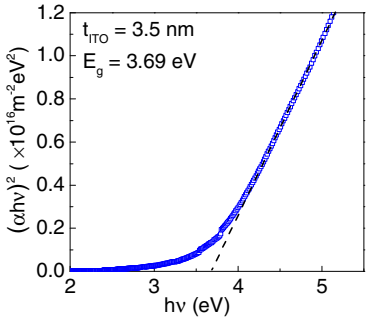

Fig. 6. Tauc plots of the 3.5-nm ITO film showing a bandgap of 3.69 eV.

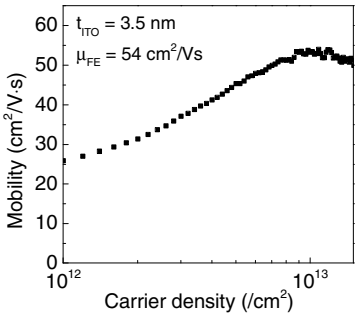

Fig. 7. The mobility versus carrier density for 3.5-nm ITO.

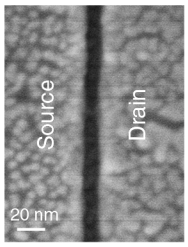

Fig. 8. SEM image of the 15-nm channel length device.

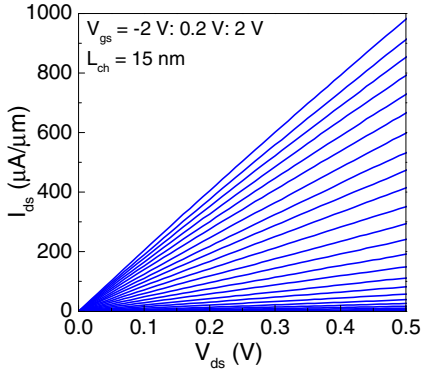

Fig. 9. Output characteristics of an ITO transistor with 15-nm channel-length.

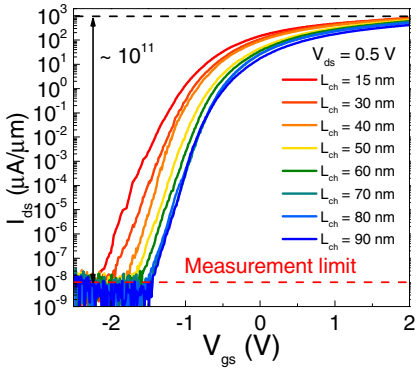

Fig. 10. Transfer characteristics of ITO transistors with different channel length.

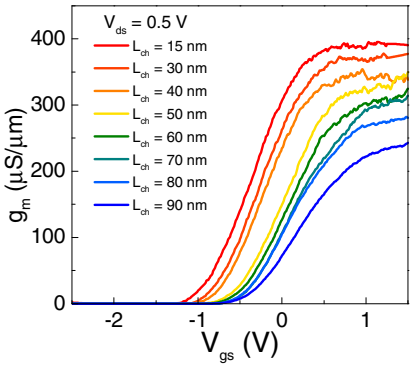

Fig. 11. g_m as a function of V_{gs} for ITO transistors with different channel-length.

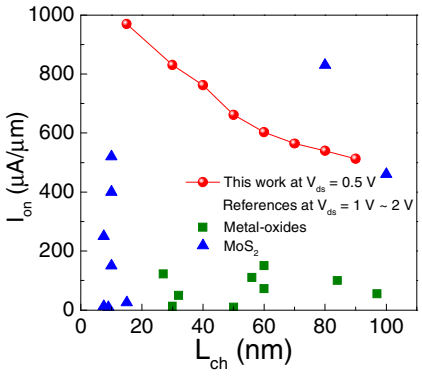

Fig. 12. Benchmark of L_{ch} dependent I_{on} for metal-oxides- and MoS_2-based transistors with ITO-based transistors.

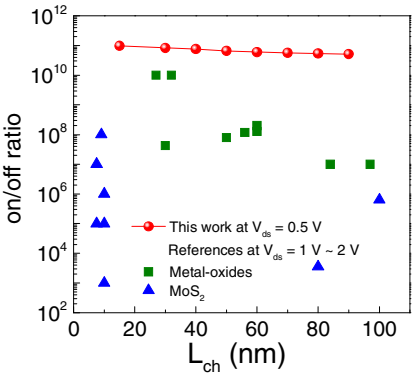

Fig. 13. Benchmarks of L_{ch} dependent on/off ratio for metal-oxides- and MoS_2-based TFTs with ITO-based transistors.

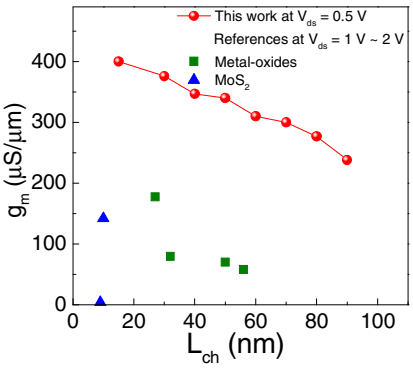

Fig. 14. Benchmarks of L_{ch} dependent g_m for metal-oxides- and MoS_2-based transistors with ITO-based transistors.

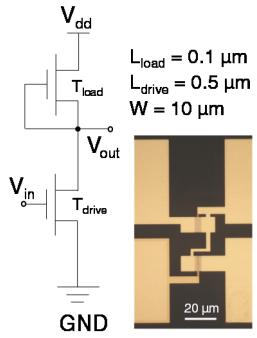

Fig. 15. The schematic and optical micrograph of the E-D mode inverter with 3.5-nm-ITO/5-nm-HfLaO transistors

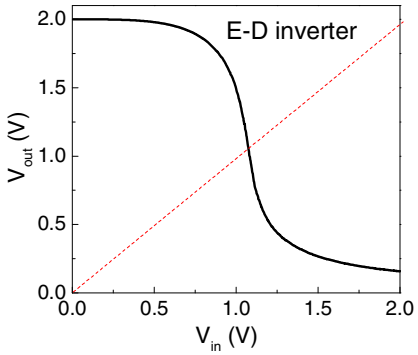

Fig. 16. The V_{in}-V_{out} characteristics of the E-D inverter with 3.5-nm-ITO/5-nm-HfLaO transistors.

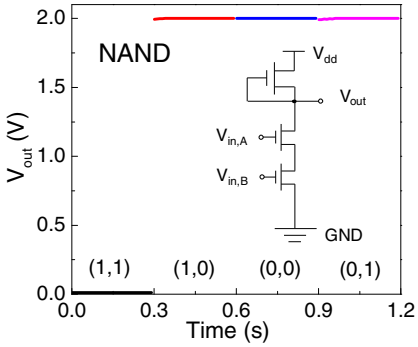

Fig. 17. The transient characteristics of the NAND logic gate with ITO-based E-D inverter.

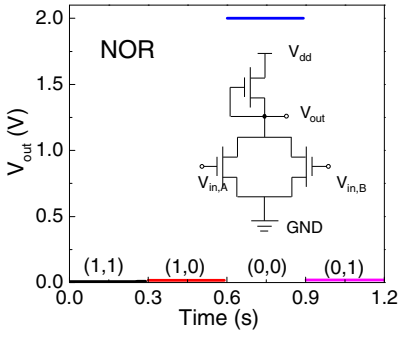

Fig. 18. The transient characteristics of the NOR logic gate with ITO-based E-D inverter.

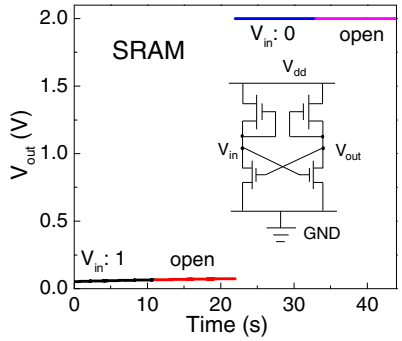

Fig. 19. The transient characteristics of the SRAM with ITO-based E-D inverter.

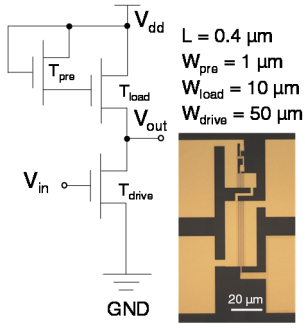

Fig. 20. The schematic and optical micrograph of BST mode inverter with 3.5-nm-ITO/5-nm-HfLaO transistors.

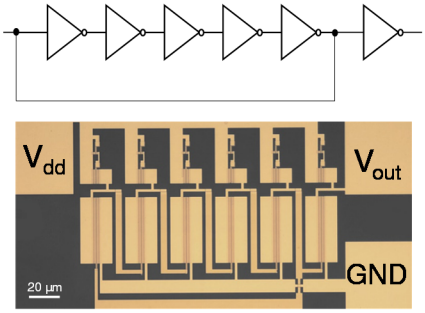

Fig. 21. The schematic and optical micrograph of 5-stage ring oscillator with ITO-based BST inverter.

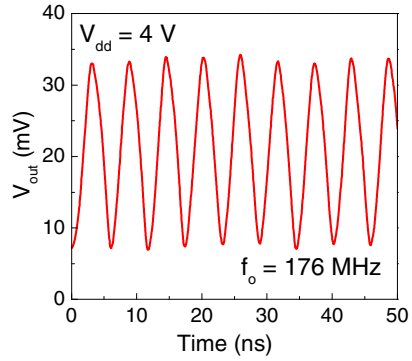

Fig. 22. The transient characteristics of the 5-stage ring oscillator based on BST inverter at V_{dd} = 4 V.

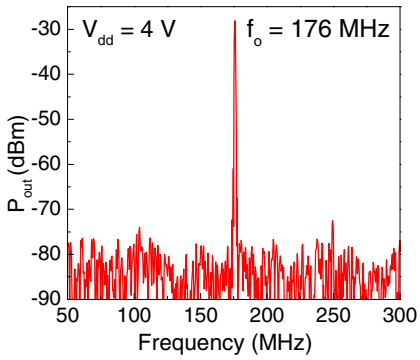

Fig. 23. The output frequency spectrum of the 5-stage ring oscillator based on BST inverter at V_{dd} = 4 V.

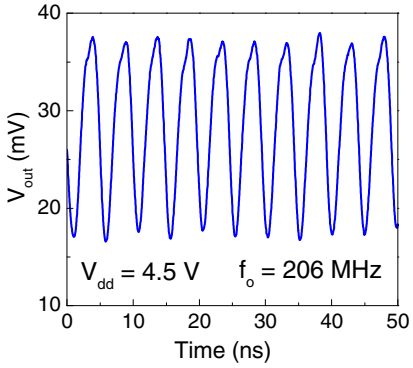

Fig. 24. The transient characteristics of the 5-stage ring oscillator based on BST inverter at V_{dd} = 4.5 V.

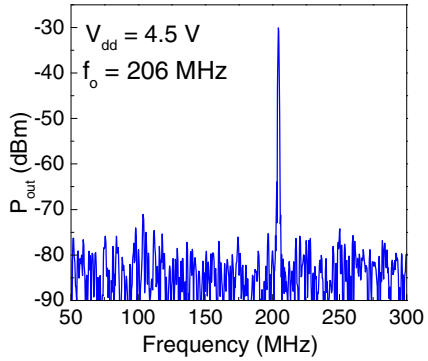

Fig. 25. The output frequency spectrum of the 5-stage ring oscillator based on BST inverter at V_{dd} = 4.5 V.

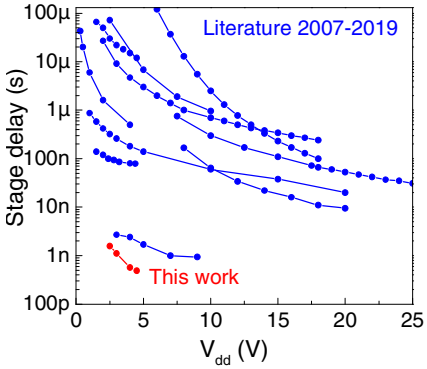

Fig. 26. Comparisons of stage delay among all metal-oxides-based ring oscillators reported to date.