Optimized Transport of Black Phosphorus Top Gate Transistors Using Alucone Dielectrics

Xuefei Li, Xiong Xiong, Tiaoyang Li, Tingting Gao, and Yanqing Wu

***Abstract*— In this letter, we demonstrate high performance black phosphorus (BP) top gate transistors using molecular layer deposition (MLD) of high-quality alucone films as top gate dielectrics. Ethylene glycol was used as an oxygen precursor instead of using water or ozone as precursor, which typically results in the oxidation of BP surface. The carrier mobility of BP transistors using the alucone dielectric reaches 216 cm^2/V·s at room temperature, which is 4.5 times higher than that of with Al_2O_3 dielectrics using O_3. The ON current and ON–OFF ratio of the alucone-based transistors are also much higher than the other two types of devices. Meanwhile, we observe a metal-insulator transition in the BP top gate with alucone films, suggesting an excellent interface quality with efficient electro-static gate control. This result shows great potential of MLD for applications in high-quality BP top gate devices.**

***Index Terms*— Black phosphorus, top gate, molecular layer deposition, alucone, mobility.**

I. Introduction

RECENTLY, the discovery of excellent transistor performances of black phosphorus (BP) has stimulated widespread research interest [1]–[11]. The development of top-gated BP FETs is of great importance for practical application. Atomic layer deposition (ALD) is a common technique for deposition high-k gate dielectrics which typically adopts water as an oxygen precursor [5]–[8]. However, black phosphorus is known to the easy formation of PO_x interfacial layer among moisture and oxygen, which will lead to significant degradation of the electronic properties of BP FETs [7], [12], [13]. As a result, the oxygen precursor using water cannot be readily adopted for top gate dielectrics on BP. Therefore, the integration of high-quality dielectrics on BP is a significant challenge that remains to be solved. Molecular layer deposition (MLD) technique is a vapor-deposition process similar to ALD based on sequential, self-limiting surface reactions for the growth of organic/hybrid organic-inorganic polymers at the molecular level, which provides precise control over thickness, composition, morphology, and conformality [14]–[16]. Instead of using water or ozone, oxygen sources in MLD are usually organic, e.g., diol, dicarboxylic acid, or diamine. Therefore, it is believed that the polymer films deposited by MLD could reduce the oxidation of BP surface and improve the electrical properties of BP FETs.

In this letter, we investigated high performance BP top-gate transistors with alucone dielectrics. Alucone is deposited by MLD using trimethylaluminum (TMA) as metal precursors and ethylene glycol (EG) as an oxygen precursor. The mobility of top-gated BP transistor with alucone dielectrics is 4.5 times higher than that of with Al_2O_3 by ALD using O_3, up to 216 cm^2/V·s, which is mainly attributed to effectively protect the surface of BP and minimize the oxidation effect of the BP surface compared with O_3 and H_2O.

II. Device Fabrication and Dielectric Deposition

Layered BP flakes were mechanically exfoliated from bulk crystal (smart elements) and then transferred onto a Si substrate covered with a 30-nm HfSiO dielectric layer. In this experiment, we compared three different oxygen sources for the top gate dielectrics: O_3, water (H_2O), and ethylene glycol (EG). (i) A 15 nm Al_2O_3 was deposited by ALD at 120 °C using trimethylaluminum (TMA) and O_3. Pulse times were 0.5 and 1 s for TMA and O_3, and purge times were 10 and 1 s, respectively. (ii) A 15 nm Al_2O_3 was deposited by ALD at 120 °C using TMA and water. Pulse times were 0.5 and 1 s for TMA and water, and purge times were 10 and 1 s, respectively. (iii) First, 5 nm alucone was deposited by MLD at 120 °C. The TMA and EG pulse times were 0.5 and 0.5 s, respectively. The purge time of each precursor was 10 and 10 s, respectively. Then, 10 nm Al_2O_3 was in situ deposited by ALD at 120 °C using TMA and water to form a 15-nm stacked alucone/Al_2O_3. Pure N_2 (99.999%) was used as carrier gas and purge gas. Finally, the top gate regions were defined by e-beam lithography. E-beam evaporated Ni/Au of 20/60 nm was deposited as the top gate metal and contacts. Electrical measurements were carried out with an Agilent B1500A semiconductor parameter analyzer and Lakeshore cryogenic probe station in vacuum ($< 10^{-5}$ Torr).

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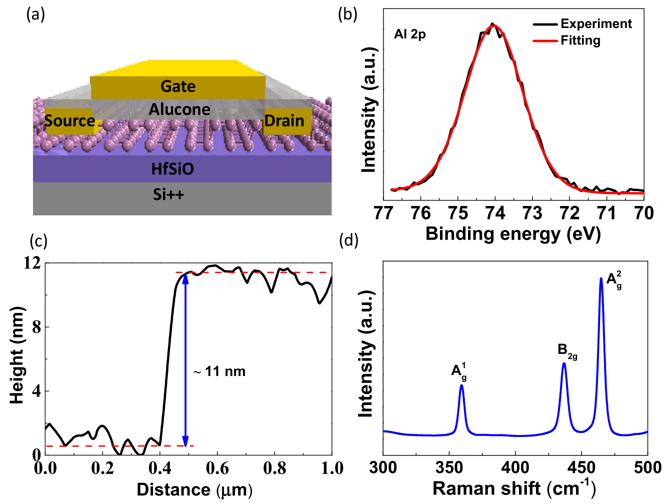

Fig. 1. (a) Schematic view of the device fabricated in this work. (b) XPS spectra in the Al 2p region for alucone MLD films. (c) BP thickness measured by AFM is 11 nm. (d) Raman characterization of the BP film along the armchair direction.

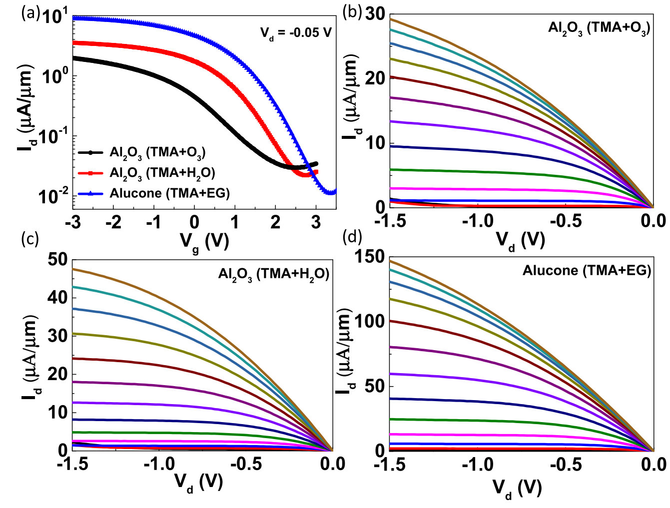

Fig. 2. (a) Transfer characteristics of the BP top-gate FET at $V_d = -0.05$ V for three different gate dielectrics at room temperature. Output characteristics of the top-gated BP devices with 15 nm Al_2O_3 by TMA + O_3 (b) and 15 nm Al_2O_3 by TMA + H_2O. (c) V_{tg} varies from 3 V to −3 V with a step of −0.5 V. (d) Output characteristics of the top-gated BP devices with alucone/Al_2O_3 (5/10 nm). V_{tg} varies from 3 V to −3 V with a step of −0.5 V. The gate length is 2 μm.

III. Device Electrical Characterization

Fig.1a displays a schematic view of a representative dual-gated BP transistor with alucone as a top-gate dielectric. Fig. 1b shows X-ray photoelectron spectroscopy (XPS) spectrum for the Al 2p peak for alucone MLD films. The Al 2p peak was observed at ~74 eV, which is consistent with the previous study [15]. The flakes were identified by a combination of optical and atomic force microscopy (AFM). A typical few-layer BP flake was confirmed to be ~11 nm by AFM as shown in Fig. 1c. BP samples with similar thickness (~11 nm) along armchair direction were carefully selected for three types of top-gated BP devices. Raman spectra were used to characterize the crystal orientations of BP material with a laser source of $\lambda = 532$ nm and 25 mW at a diameter of the laser spot of 2 μm as shown in Fig.1d. The three characteristic Raman modes, A_g^1, B_{2g}, and A_g^2, can be observed, corresponding to the out-of-plane vibration (~ 361 cm^{-1}), in-plane vibration along the zigzag (~438 cm^{-1}) and armchair (~ 466 cm^{-1}) directions, respectively [9], [10]. The transistors were fabricated along the light effective mass (armchair-) direction of the BP film to achieve the highest electrical performance.

Fig. 2a shows the transfer characteristics of top gate BP FETs with three different dielectrics at room temperature. It is clear that the device with alucone exhibits the highest drain current and on-off ratio. The equivalent oxide thickness (EOT) of alucone/Al_2O_3 (5/10 nm) dielectric is 8.7 nm, corresponding to a dielectric constant of 6.7. It should be noted that both of the thickness of alucone and Al_2O_3 could be further reduced by decreasing the MLD/ALD cycles to achieve sub-5-nm stacked alucone/Al_2O_3. The field-effect mobility of the top-gate device with alucone is 216 cm^2/V·s, which is a factor of 4.5 and 2.1 larger than that in devices with Al_2O_3 dielectrics using O_3 and H_2O, respectively. Fig. 2b-d compare the output characteristics of top-gated BP devices. The maximum drain current at $V_{tg} = -3$ V and $V_d = -1.5$ V for the devices with Al_2O_3 dielectrics using O_3 or H_2O as well as alucone at room temperature is 29, 48, and 149 μA/μm, respectively. It is expected because the introduction of H_2O can result in the oxidation of BP during deposition oxide. Meanwhile, O_3 is a strong oxidant and causes the severe oxidation of the BP surface. The formation of PO_x interfacial layer between dielectrics and BP can strongly degrade the electrical properties of BP [17]. On the contrary, BP is stable in the ambient of EG, which protects the surface and preserves the semiconductor properties of BP.

To investigate the role of V_{bg} on the electrical properties of top gate BP FETs, the transfer characteristics of the alucone devices at various V_{bg} with $V_d = -0.05$ V are shown in Fig. 3a. With decreasing V_{bg} from 2 to −3 V, the transfer curve moves towards more positive voltages, indicating a p-type doping effect. Fig. 3b shows the contour plot of I_d as a function of V_{tg} and V_{bg} at 300 K with V_d fixed at −0.05 V. It is found that the I_d depends on both of V_{tg} and V_{bg}. We extract the values of V_{tg} and V_{bg} for $I_d = 5$ μA/μm as shown in Fig. 3c. It is evident that V_{bg} is linear with V_{tg} and the slope is ~ 1.33. This is consistent with the value of $EOT_{top-gate}/EOT_{back-gate}$, where the EOT of alucone/Al_2O_3 top-gate dielectric stack and back-gate HfSiO are 8.7 and 6.5 nm, respectively [18].

The transfer characteristics of the alucone device at $V_d = -0.05$ V from 300 to 4.3 K are plotted in Fig. 4a. A clear metal-insulator transition (MIT) is observed and the crossing point is independent of the temperature and locates at a well-defined point $V_{tg} = 0.7$ V, which indicates an excellent interface quality [19]. It should be noted that previous such signature of MIT is demonstrated mostly in back-gated devices [10]. In order to study the Schottky barrier height, we fit the data at $V_d = -0.05$ V to the classical thermionic emission equation of Schottky barriers. Fig. 4b shows the Arrhenius plot of $\ln(I_d/T^{3/2})$ versus 1000/T for various values

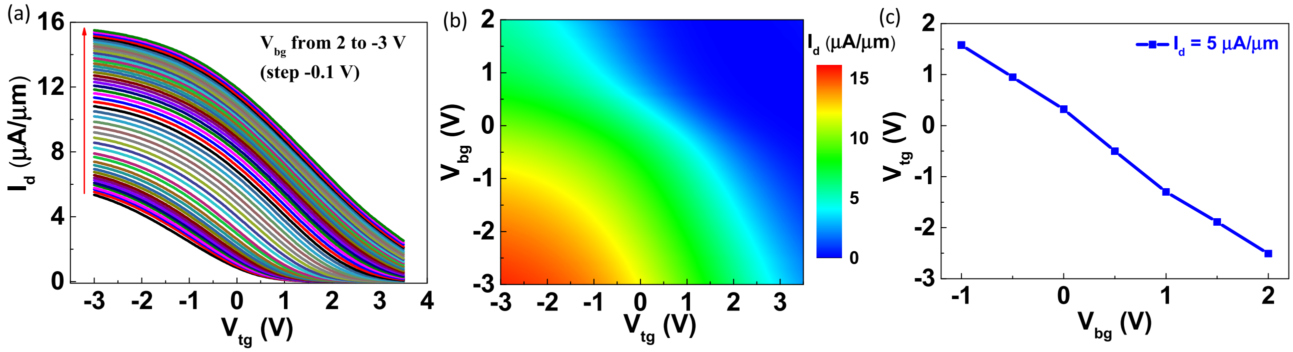

Fig. 3. (a) $I_d - V_{tg}$ characteristics of BP dual-gate FET with alucone dielectrics at $V_d = -0.05$ V while changing V_{bg} from 2 to -3 V with a -0.1 V step at 300 K. (b) Contour plot of drain current I_d (μA/μm) as function of V_{bg} and V_{tg} at room temperature. (c) The linear relation between V_{bg} and V_{tg} at 300 K.

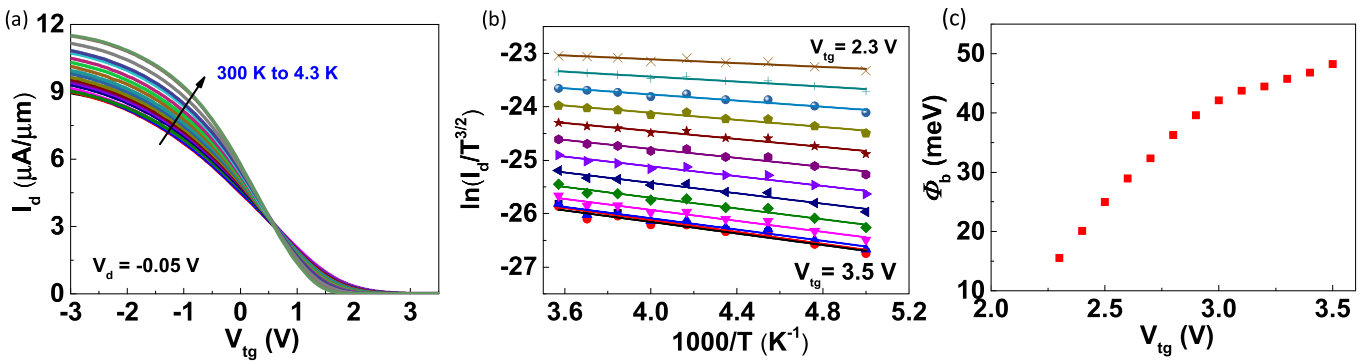

Fig. 4. (a) Transfer characteristics of the top-gated BP device with alucone from 300 to 4.3 K at $V_d = -0.05$ V. V_{bg} is fixed at 0 V. (b) Arrhenius plot of the conductance of top-gated BP with alucone dielectrics. (c) Dependence of Φ_b on V_{tg}.

of V_{tg} from 3.5 to 2.3 V [10]. It is clear that the thermally activated behavior fits the data very well from 300 to 200 K, with extracted Schottky barrier height Φ_b shown in Fig. 4c. The Schottky barrier height of Ni-BP contact decreases from 48.3 to 15.5 meV with the top-gate voltage changing from 3.5 to 2.3 V.

IV. Conclusion

In conclusion, we have investigated the electrical properties of black phosphorus top gate transistors with three different dielectrics. Compared to the Al_2O_3 deposited using H_2O or O_3, the alucone polymer films exhibit the best interface quality with BP. The improvement in mobility is mainly attributed to the effective suppression of the surface oxidation of the BP channel, which provides a new route to realizing high performance BP top gate devices.

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